CONFIDENTIAL B

MT6765 PCB Design Guidelines V0_1

2017/11/24

Revision History

Version	Date	Description	Editors
V0_1	2017/11/24	First release	Mavis Wang, Ivy Hsiao, Wanda Tseng, Zuoru Yi, YH Ku , PH Chang , PS Chen, FK Pan, Charles Chen

Outlines

- **Packaging**
  - Package outline of MT6765
  - MT6765 footprint recommendation
  - MT6765 ball out design
- **General Guidelines**
  - PCB stack-up recommendation
  - Placement notes
- **Design Guidelines for High-speed Digital Signals**
  - LPDDR4X/LPDDR3
  - PDN design
- **Others**
  - MT6765 RF interface - MT6177 (RF transceiver)
  - MT6765 RF interface - MT6177M (RF transceiver)
  - MT6357 (PMU)
  - MT6631 (BT/FM/Wi-Fi/GPS)
  - MT6371 (battery charger/USB_PD)
  - eMMC/USB/MIPI/SIM card/T-card

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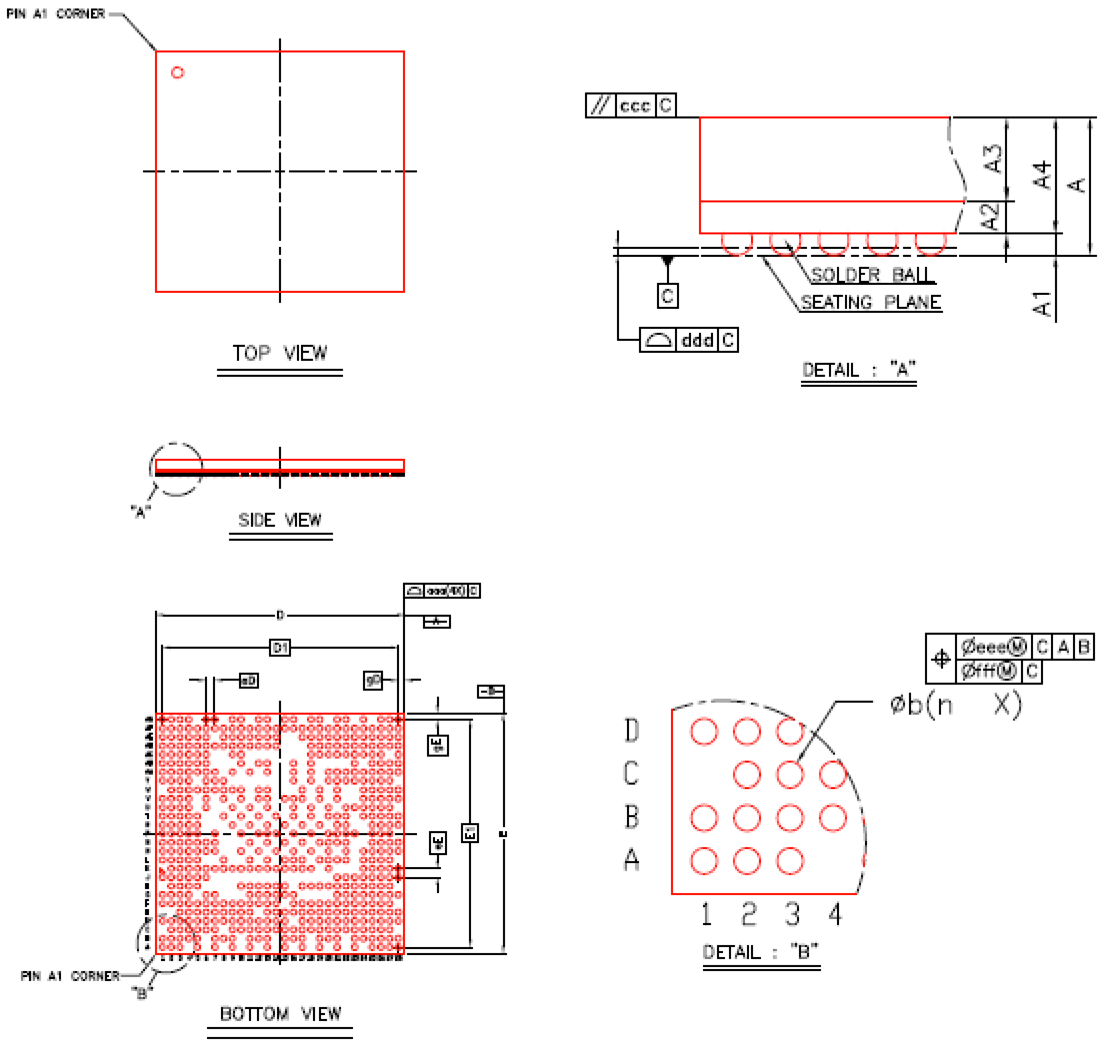
Package Outline of MT6765



Item		Symbol	Common Dimensions		
			MIN.	NOM.	MAX.
Package Type			MFC VFBGA		
Body Size	X	D	11.3	11.4	11.5
	Y	E	10.9	11.0	11.1
Ball Pitch	X	eD	0.40		
	Y	eE	0.40		
Mold Thickness		A3	0.45 Ref.		
Substrate Thickness		A2	0.141 Ref.		
Substrate+Mold Thickness		A4	0.541	0.591	0.641
Total Thickness		A	–	–	0.90
Ball Diameter			0.25		
Ball Stand Off		A1	0.14	0.18	0.22
Ball Width		b	0.22	0.27	0.32
Package Edge Tolerance		aaa	0.05		
Mold Flatness		ccc	0.10		
Coplanarity		ddd	0.08		
Ball Offset (Package)		eee	0.15		
Ball Offset (Ball)		fff	0.05		
Ball Count		n	558		
Edge Ball Center to Center	X	D1	10.80		
	Y	E1	10.40		
Edge Ball Center to Package Edge	X	gD	0.30		
	Y	gE	0.30		

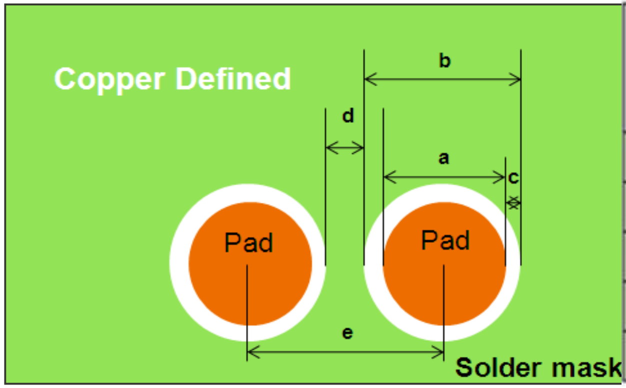
MT6765 Footprint Recommendation

Note:

- Use **copper defined** for all solder pads (see Figure 1).
- Recommended stencil opening ➔ 0.24mm square with 0.075R angle (see green area in Figure 2)
- **Use 0.1/0.22mm (drill/land) laser via on PAD to improve the yield of SMT.**

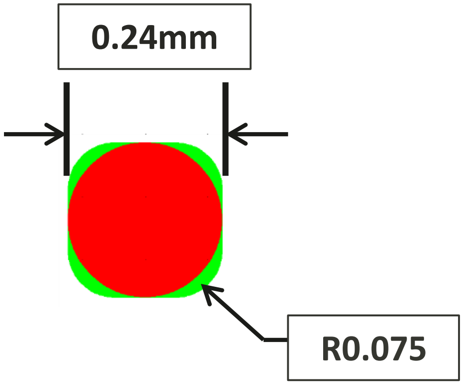
As in Figure 1, use **copper defined** for all pins.
Pad size: 0.24mm; solder mask: 0.315mm

Figure 1

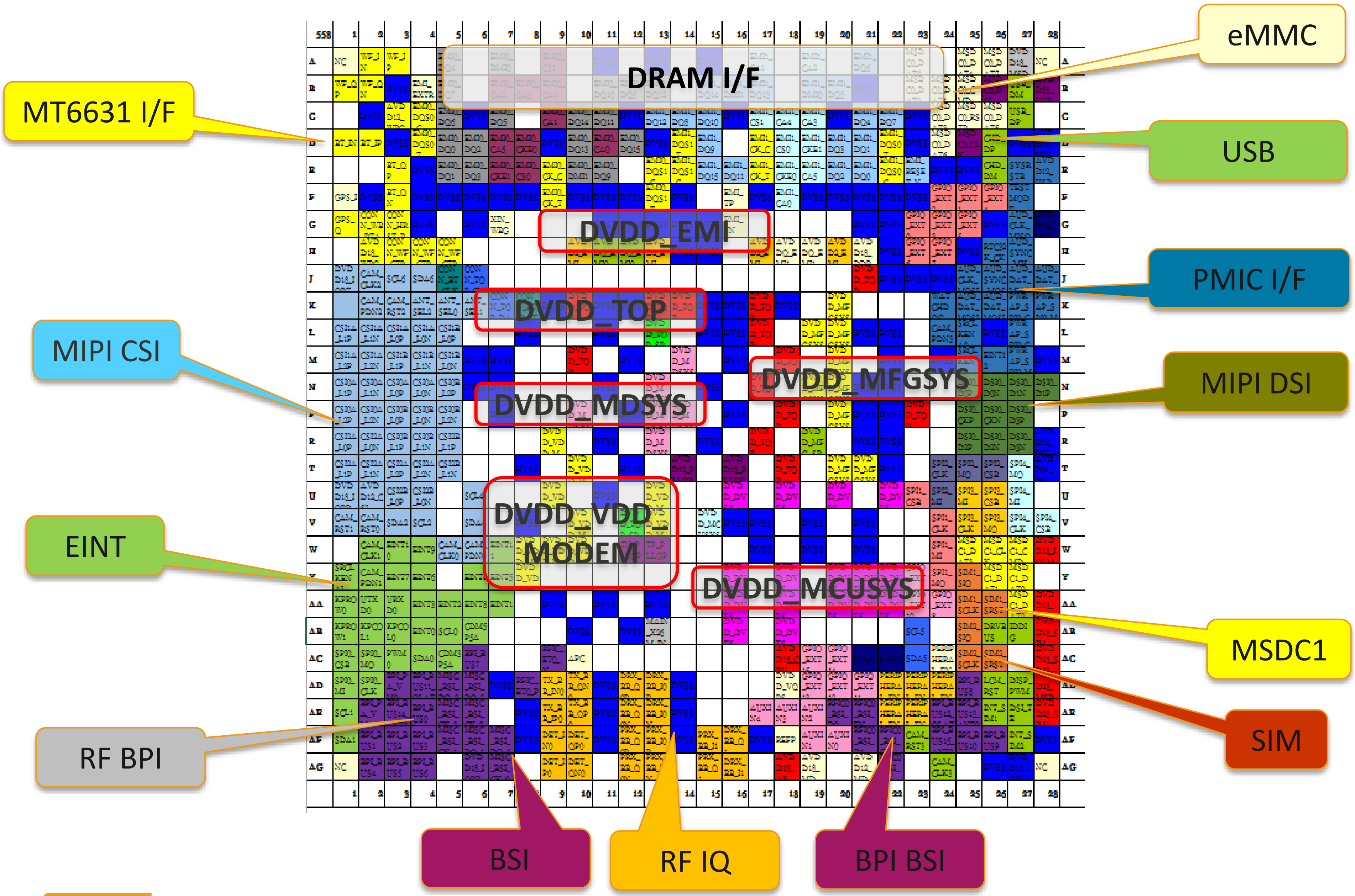


Copper defined PCB land pad and Solder mask opening rule		
Land pad size	a	0.24mm
Sloder mask opening	b	a+0.075mm
Solder mask clearance	c	0.0375mm
Solder dam	d	0.085mm
Ball pitch	e	0.4mm

Figure 2



MT6765 Ball Out Design



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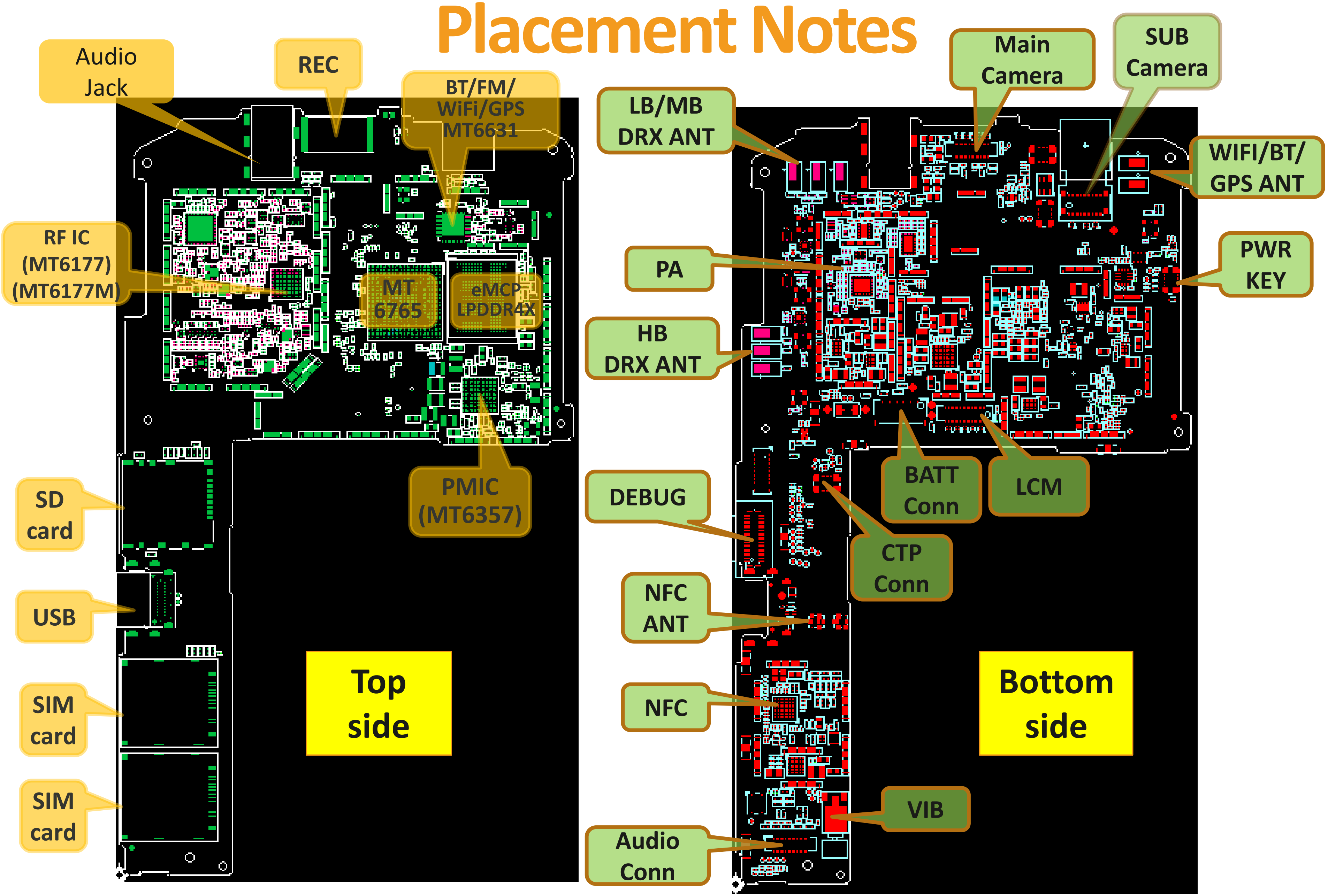
PCB Stack-up Recommendation

- To keep the best power integrity, select PCB with thinner thickness, $\leq$ 0.8mm.
- Follow the relative stack-up arrangement listed on the following pages for LPDDR4X and power distribution network.
- Others signals can be routed in the rest of the area.
- PCB stack-up is recommended here. For other combinations, extend from them.
  - 8 layer HDI2

PCB Stack-up: 8-layer HDI2

Layers	Stack-up	HDI-2 (2-6-2)				Layer definition Signal/Power/Ground (S/P/G)		
		Theoretic thickness (um)	Theoretic thickness (mil)	Material	ER	LPDDR3	LPDDR4X	Power
SR		20	0.79	SR	3.4~3.6			
L1		25	0.98	Copper		S	S	
		60	2.36	Prepreg	3.4~3.6			
L2		19	0.75	Copper		G	G	
		60	2.36	Prepreg	3.2~3.4			
L3		22	0.87	Copper		S	S	G
		75	2.95	Prepreg	3.2~3.4			
L4		15	0.59	Copper		P	G	G
		305	12.0	Core	3.2~3.4			
L5		15	0.59	Copper		G	P	G
		75	2.95	Prepreg	3.2~3.4			
L6		22	0.87	Copper				P/G
		60	2.36	Prepreg	3.2~3.4			
L7		19	0.75	Copper				P
		60	2.36	Prepreg	3.4~3.6			
L8		25	0.98	Copper				
SR		20	0.79	SR	3.4~3.6			
	Total	0.897 mm ±10%	35.3 mil ±10%					

Placement Notes



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PCB Module Design

MMD
MediaTek Module Design

- **We recommend you adopt modules by MediaTek as the first priority.**

As the design trend turns to developing light, thin and higher battery capacity on smart phones, the complexity on system design becomes a great challenge nowadays. It is a time and cost consuming process to meet the layout constraints and at the same time deliver a good signal and power integrity.

To help our customers to rapidly design a correct, performance-oriented and reliable layout on PCB, we have introduced the **MMD (MediaTek Module Design)** solution. MMD provides optimized CPU and MCP layout design with guaranteed performance and stability. Meanwhile, it greatly shortens the time to market.

The main purpose of MMD is providing a convenient and flexible solution. The ideal condition is to implant the modules without any modification. However, if the module cannot match your mechanics, you can still partially adopt MMD and enjoy the benefits from it.

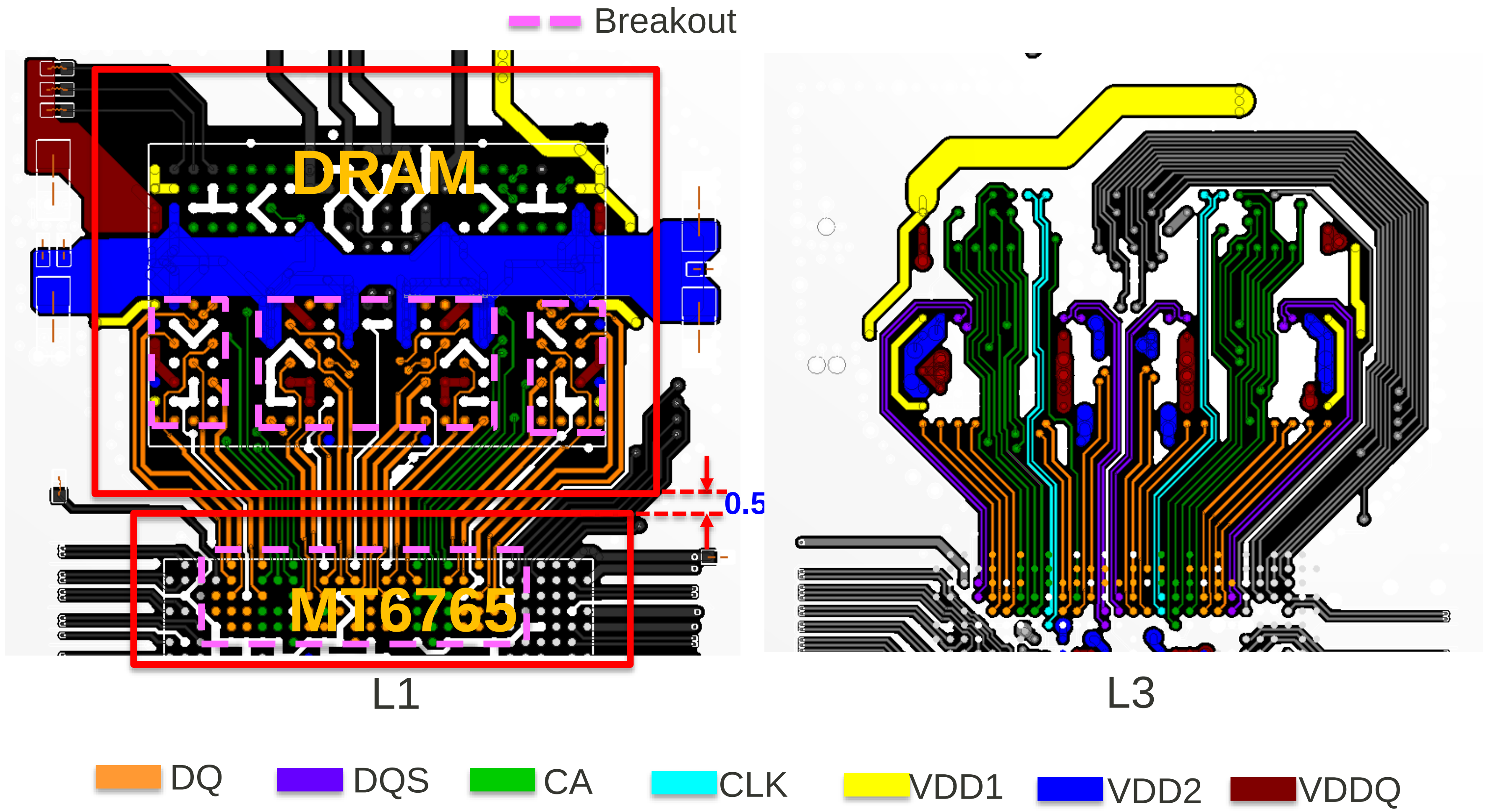
Contact your corresponding FAE when you have any problem in introducing MMD.

Enabling your High-speed Digital Design~

SIE (Signal Integrity Express): SI/PI simulation support

LPDDR4X - Placement

- Please keep the spacing between MT6765 and DRAM as small as possible.
- Recommend the spacing is less than 0.5mm.



PCB Design Guidelines for LPDDR4X (I)

Grouping	Signal Name	#	Description
DQ	EMI[0:1]_DQ[0:15]	32	Data bus
	EMI[0:1]_DMI[0:1]	4	Data mask
CA	EMI[0:1]_CA[0:5]	12	Command/Address
	EMI[0:1]_CKE[0:1], EMI[0:1]_CS[0:1], EMI_RESET_N	9	Clock enable, Chip select, Reset
DQS	EMI[0:1]_DQS[0:1]_T, EMI[0:1]_DQS[0:1]_C	8	Data strobe
CLK	EMI[0:1]_CK_T, EMI[0:1]_CK_C	4	Clock

- Please remove test point if not necessary
- Place ground via when layer transition happens
- For **LPDDR4X-3200 Mbps**, it is recommended that the thickness of **Prepreg1-2 and Prepreg2-3** are less than **60um**.
- It is not necessary to match DQ/CA routing length but keeping trace length as short as possible.
- DQ with 40~50Ω characteristic impedance is suggested.
  - Keep the same center-to-center spacing for isolation consideration.
- Length matching on DQS/CLK
  - |EMI[0:1]_DQS[0:1]_T-EMI[0:1]_DQS[0:1]_C| < 150um
  - |EMI[0:1]_CK_T-EMI[0:1]_CK_C| < 150um
- Channel length table

	EMI[0:1]_DQ[0:7] EMI[0:1]_DMI0	EMI[0:1]_DQ[8:15] EMI[0:1]_DMI1	CA	CKE/CS	DQS	CK
Max. Length (mm)	11.5	9.5	13	15	14	14

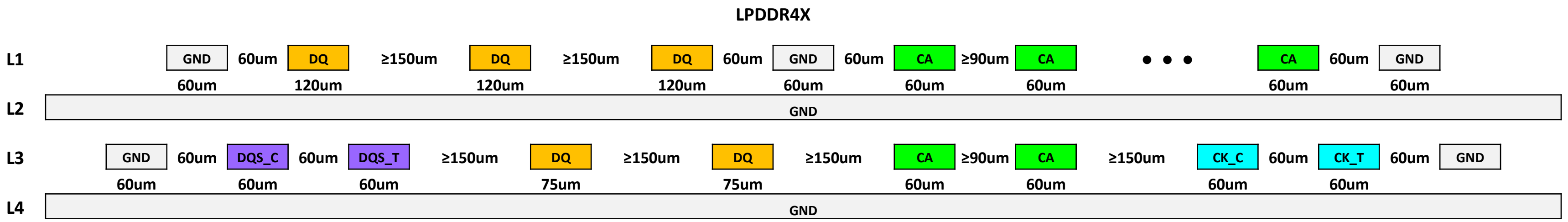
PCB Design Guidelines for LPDDR4X (II)

➢ Keep solid L2&L4 reference plane (GND)

- For DQ/CA at L1, refer to ground beneath
- For DQ/CA/CLK/DQS at L3, refer to ground plane both above and below

➢ Signals layout topology should be routed at L1 and L3 as illustrated below

- For DQ routing at L1, three signal traces with adjacent GND shielding are suggested
  - GND Shielding traces at L1 must connect to ground plane at L2 through ground via and/or ground balls at L1 at both SoC side and DRAM side.
- For CA routing at L1, five signal traces become a group with nearby GND shielding
- For DQ/CA/CLK/DQS at L3, signal traces with GND reference beneath are suggested



➢ Summary of the required trace width and spacing

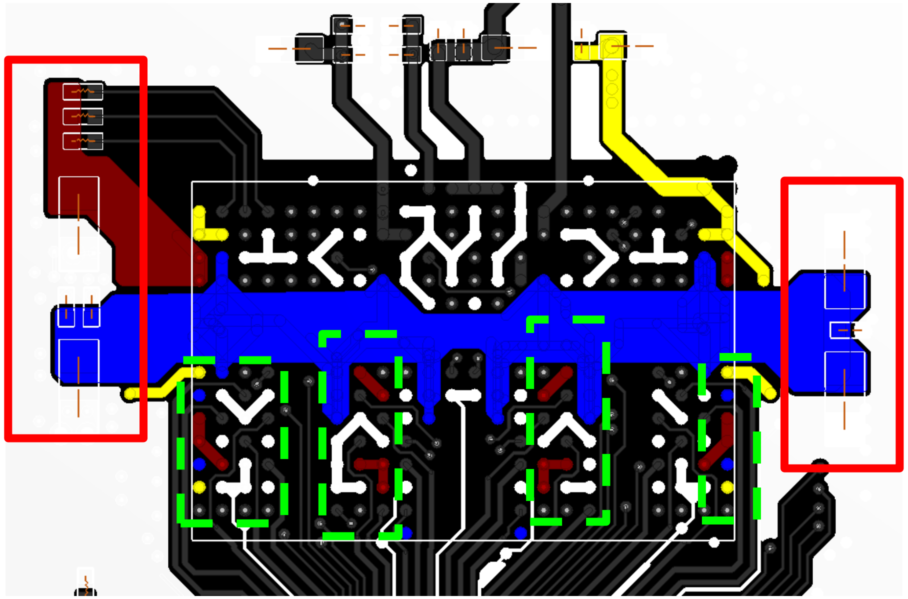
Group	Routing Layer	Reference	Shielding	Width(um)		Edge-to-edge Spacing(um)		Ground Spacing(um)
				Main Route	Breakout	Main Route	Breakout	
DQ	L1	L2	GSSSG	120	60	≥150	≥90	60
	L3	L2, L4		75	60	≥150	≥80	60
CA	L1	L2	Group	60	60	≥90	≥90	60
	L3	L2, L4		60	60	≥90	≥80	60
DQS/CLK*	L3	L2, L4		60	60	≥150	≥80	60

*** Spacing of DQS_C-to-DQS_T/CK_C-to-CK_T is 60 um**

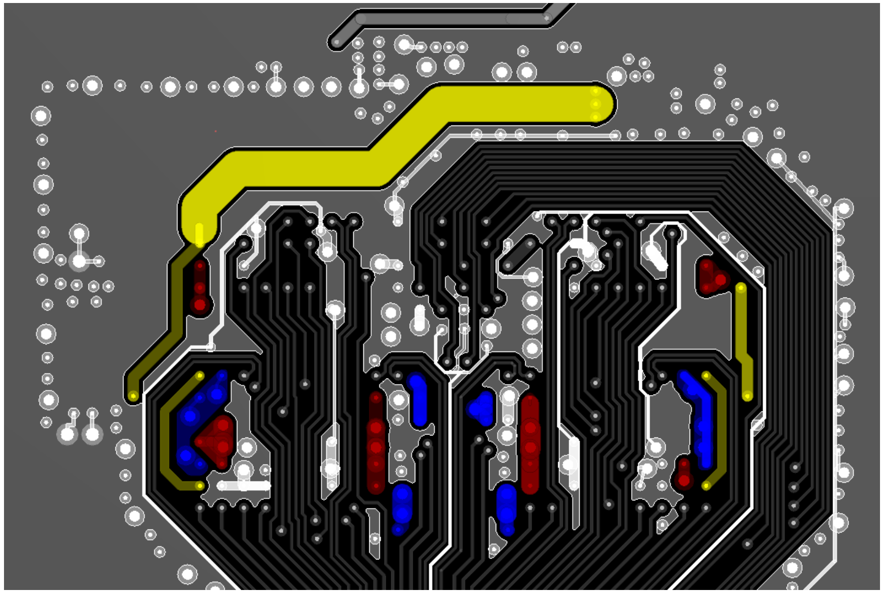
DRAM Device PDN guide line

- **2-sided SMT:**
  - Make VDD2 PWR connection at L1 and place capacitor at each side
    - Get the power trace as wide as possible (60 mil is suggested)
  - Place capacitors beneath each region for VDD1, VDD2, and VDDQ
  - For each capacitor at the back side, it requires at least 3 PTH vias
    - Place GND via as close as possible to PWR via
  - ChA/B VDD1 R_{dc} < 60 mohm
  - Adopt MMD DRAM PDN design is strongly suggested

L1



L3



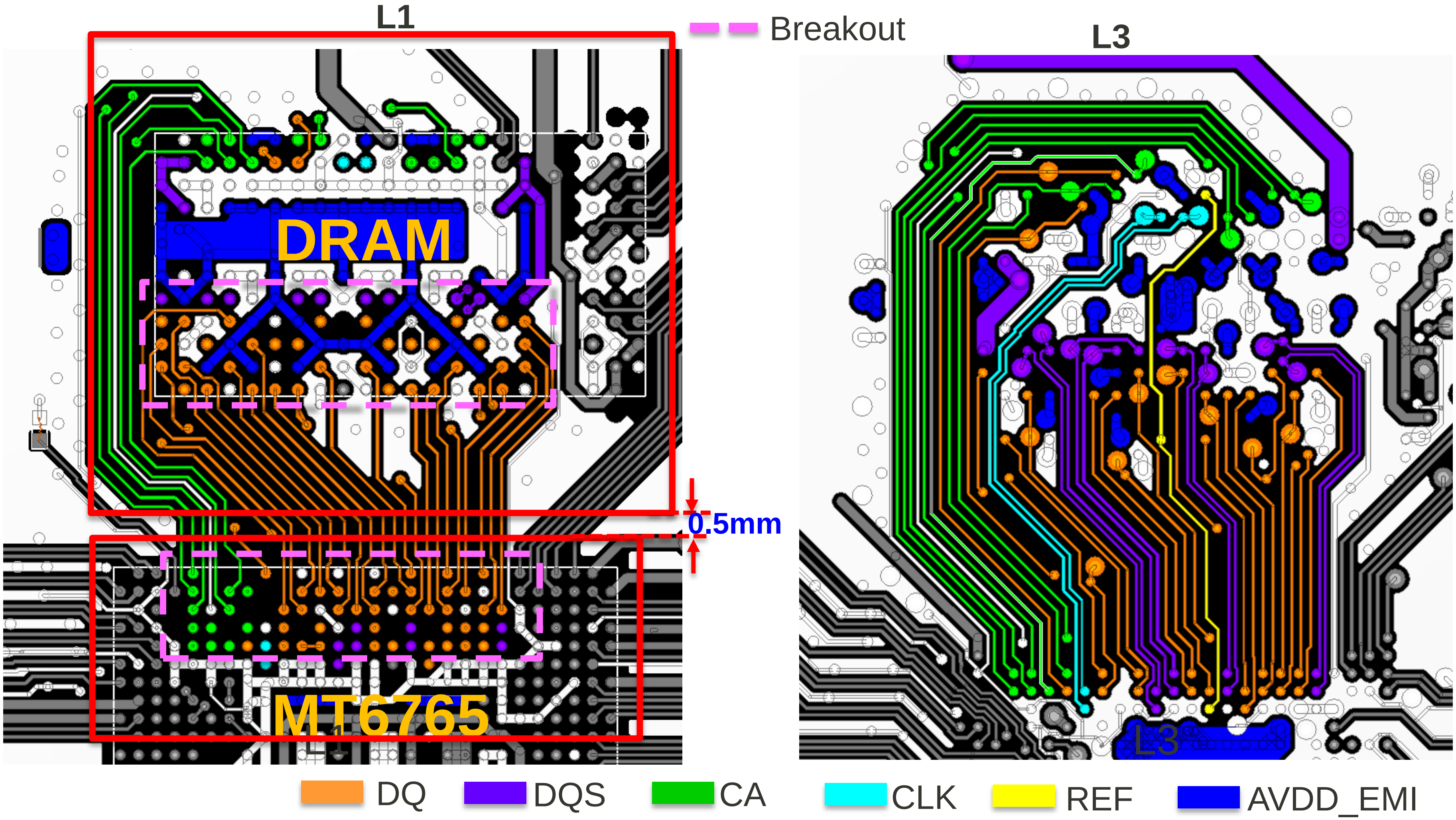
0201/0603 capacitors at the top side

0201 capacitors at the back side

VDD1 VDD2 VDDQ

LPDDR3 - Placement

- Please keep the spacing between MT6765 and DRAM as small as possible.
- Recommend the spacing is less than 0.5mm.



PCB Design Guidelines for LPDDR3 (I)

Grouping	Signal Name	#	Description
DQ	EMI0_DQ[0:31]	32	Data bus
	EMI0_DMI[0:3]	4	Data mask
CA	EMI0_CA[0:9]	10	Command/Address
	EMI0_CKE[0:1], EMI0_CS[0:1],	4	Clock enable, Chip select, Reset
DQS	EMI0_DQS[0:3]_T, EMI0_DQS[0:3]_C	8	Data strobe
CLK	EMI0_CK_T, EMI0_CK_C	2	Clock
REF	VREF_EMI	1	Reference voltage

- Please remove test point if not necessary
- Place ground via when layer transition happens
- It is not necessary to match DQ/CA routing length but keeping trace length as short as possible.
- Length matching on DQS/CLK
  - |EMI0_DQS[0:3]_T-EMI0_DQS[0:3]_C| < 150um
  - |EMI0_CK_T-EMI0_CK_C| < 150um

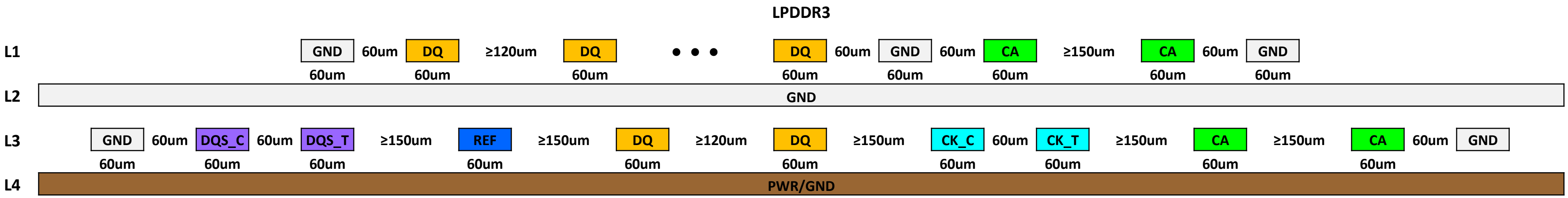
PCB Design Guidelines for LPDDR3 (II)

➢ **Keep solid L2&L4 reference plane (GND)**

- For DQ/CA at L1, refer to ground beneath
- For DQ/CA/CLK/DQS at L3, refer to ground/power plane both above and below

➢ **Signals layout topology should be routed at L1 and L3 as illustrated below**

- For CA routing at L1, two signal traces with adjacent GND shielding are suggested
  - GND Shielding traces at L1 must connect to ground plane at L2 through ground via and/or ground balls at L1 at both SoC side and DRAM side.



➢ **Summary of the required trace width and spacing**

Group	Routing Layer	Reference	Shielding	Width(um)		Edge-to-edge Spacing(um)		Ground Spacing(um)
				Main Route	Breakout	Main Route	Breakout	
DQ	L1	L2		60	60	>120	>90	60
	L3	L2, L4		60	60	>120	>80	60
CA	L1	L2	GSSG	60	60	>150	>90	60
	L3	L2, L4		60	60	>150	>80	60
DQS/CLK	L3	L2, L4		60	60	>150	>80	60
REF	L3	L2, L4		60	60	>150	>80	60

*** Spacing of DQS_C-to-DQS_T/CK_C-to-CK_T is 60 um**

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Basic Concepts of Power Delivery Network

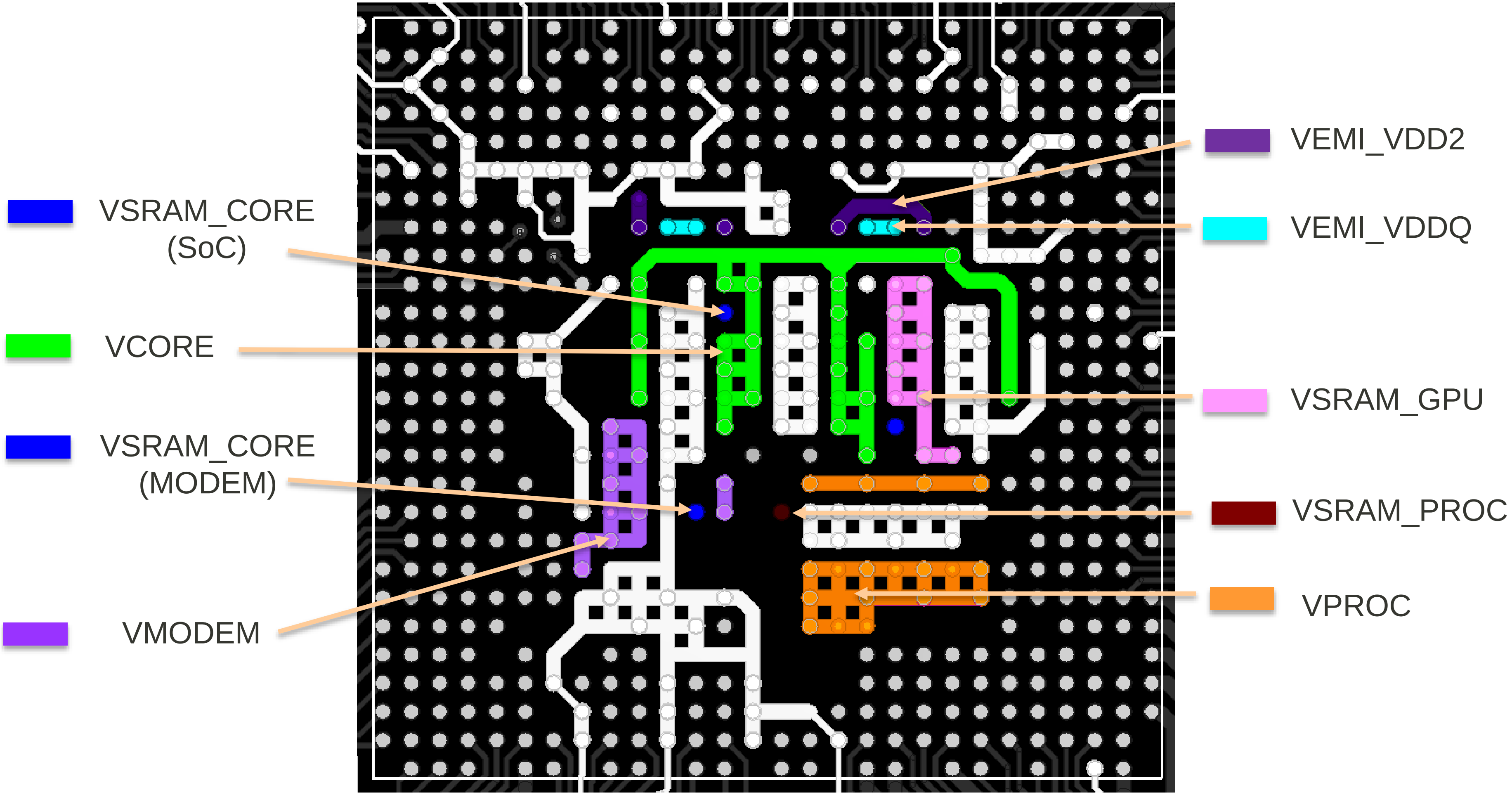
- With the increasing demand of switching current and power consumption, the conventional PCB design concept is no longer sufficient in dealing with high-performance smart phone. Thus, a well-designed PDN (Power Delivery Network) on PCB is greatly significant for system stability and performance.
- The whole PDN should include all the interconnections and current return paths from PMIC to AP. The performance mainly depends on the location and number of power traces, PWR/GND vias, and decoupling capacitors. These parameters are defined in the following guidelines.

Ball List Table

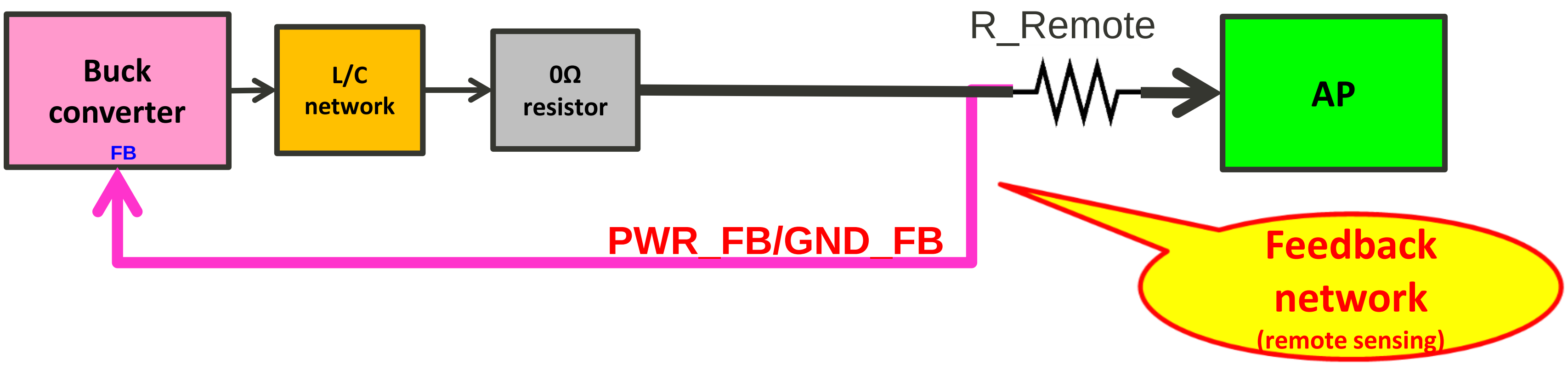
Signal Name	#	Ball	Description
VPROC **(DVDD_DVFS)**	16	U16, Y16, AA16, AB16, U18, Y18, AA18, AB18, U20, Y20, AA20, Y21, AA21, U22, Y22, AA22	Provides application processor CPU power
VGPU (**DVDD_GPU**)	9	L19, N19, K20, L20, M20, N20, P20, T20, T21	Provides application processor GPU power.
VCORE (**DVDD_CORE**)	19	P10, M10, K10, R13, P13, N13, K13, P14, M14, K14, R17, N17, L17, K17, T18, P18, M18, J21, P23	Provides application processor CORE power.
VMODEM (**DVDD_MODEM**)	10	W8, Y8, R9, U9, W9, T10, V10, W10, U13, V13	Provides application processor MODEM power.
VEMI_VDD2 (**VDD2_EMI**)	4	H10, H13, H17, H20	Provides application processor EMI VDD2 power.
VEMI_VDDQ (**VDDQ_EMI**)	4	H11, H12, H18, H19	Provides application processor EMI VDDQ power.
VSRAM_PROC (**VSRAM_PROC_PMU**)	1	V15	Provides application processor CPU SRAM power.
VSRAM_CORE (**VSRAM_OTHERS_PMU**)	3	R19, V12, L13	Provides application processor CORE SRAM power.

Decoupling Caps Placement Suggestions

To maintain power integrity, place decoupling capacitors beneath power balls.



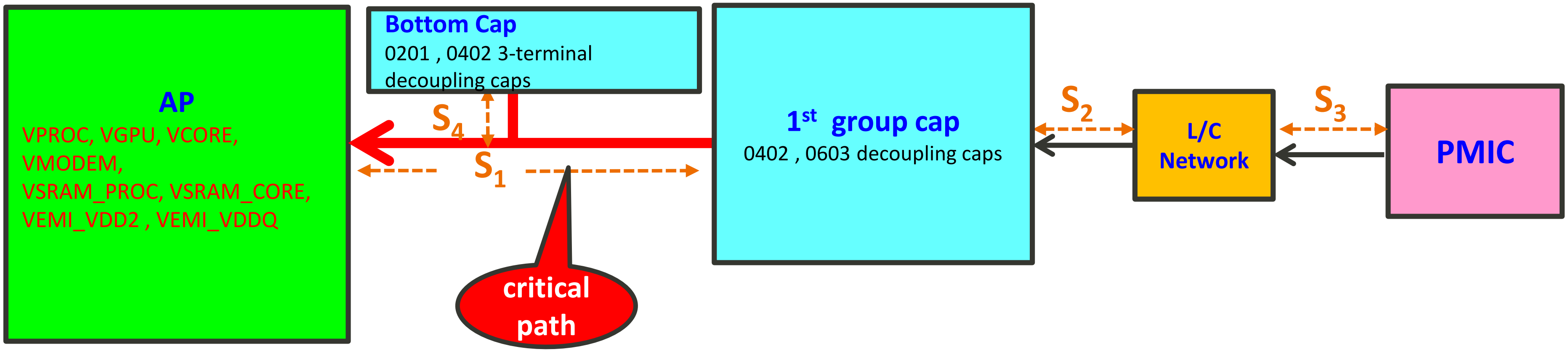
Guidelines for Remote Sensing



To compensate voltage loss, each two feedback paths (PWR_FB and GND_FB) are connected from every critical power domain which is close to MT6177 to the buck converter (PMIC).

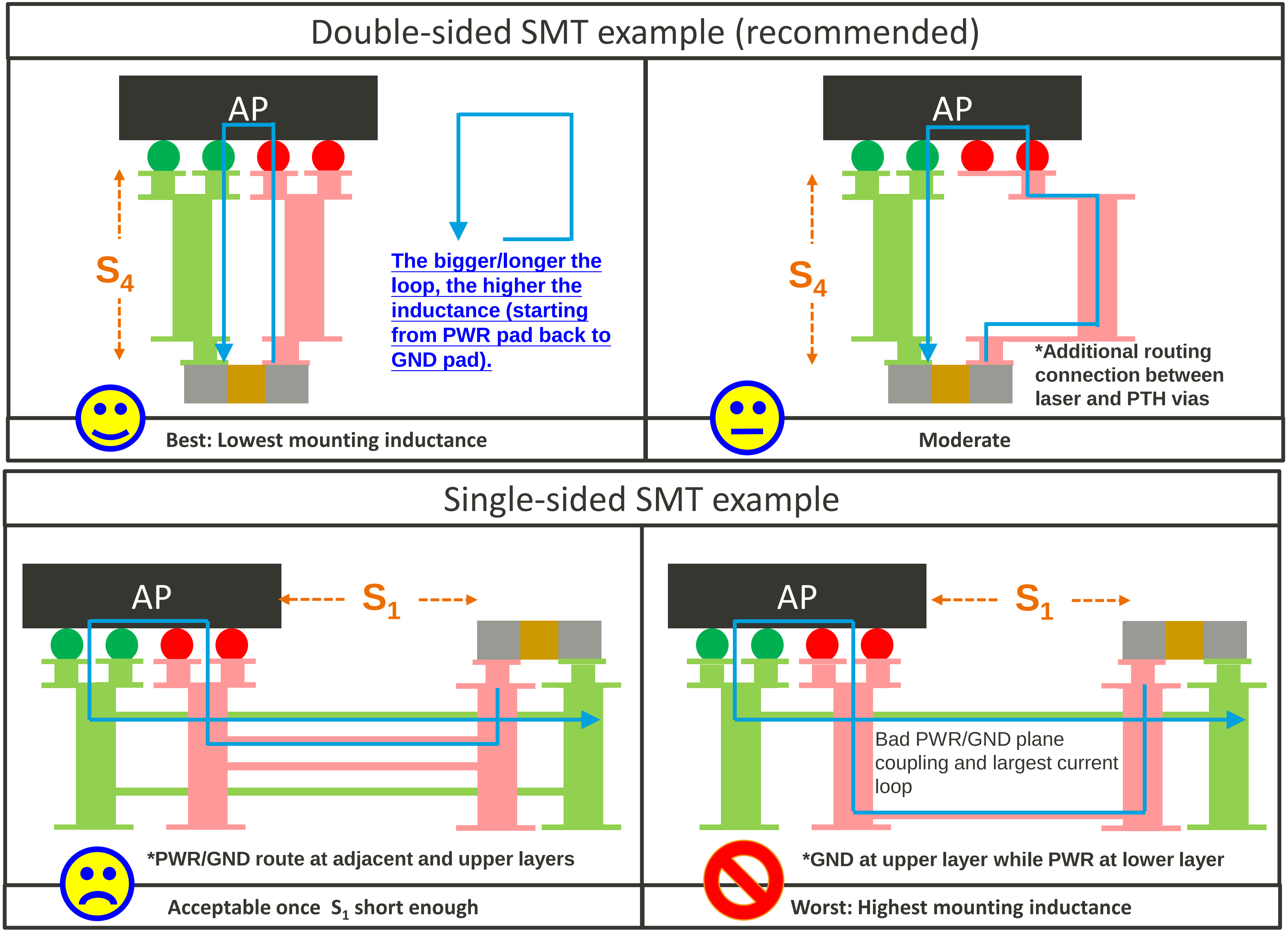
1. The voltage detection networks are sensitive to noise coupling. Use ground shielding for the entire trace including vias.
2. To keep the accuracy of feedback voltage, do not move the connection away from the bottom of AP and follow the resistance(R_Remote) spec.

Guidelines for Power Domain

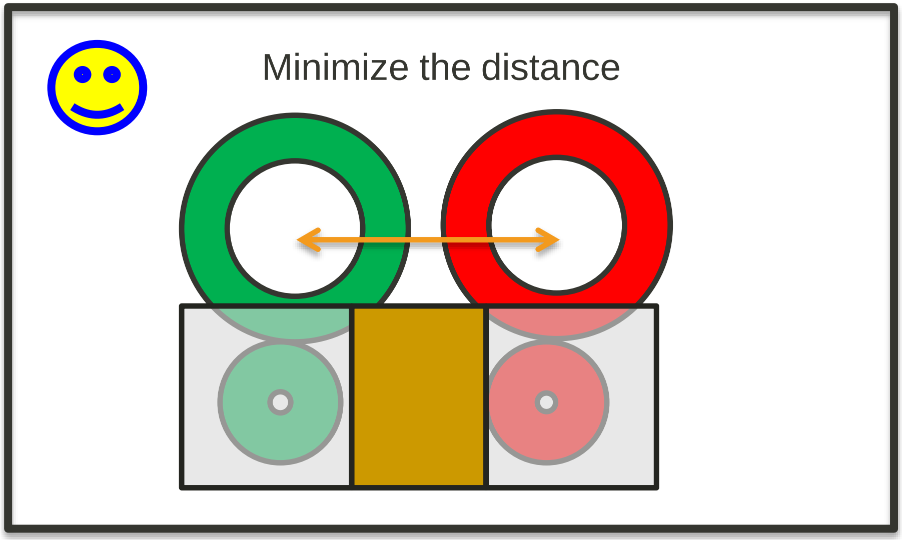


1. The whole PDN is from PMIC output pin, through (the LC low-pass filter) & decoupling caps to AP. PDN is the source of all switching currents.
2. "Critical-Path" is defined as the power trace segment from the 1st group cap to AP. The critical path design should follow the given PCB layout guidelines.
3. 2-sided SMT:
   1) In the "bottom cap" region, place 0201 and 0402 SMD capacitors right underneath the power balls. In "1st group cap" region, place the rest of decoupling caps.
   2) S_1 is defined as the critical path from "1st group cap" to AP. The corresponding PCB routing rules are given as the following (8L PCB):
      - VPROC: 1 layer PWR+1 layer GND, 9 PTH Vias, S_1 length ≤ 450mil, S_1 width ≥ 200mil. (thickness ≥ 0.6mil)
      - VGPU: 1 layer PWR+1 layer GND, 4 PTH Vias, S_1 length ≤ 450mil, S_1 width ≥ 150mil. (thickness ≥ 0.6mil)
      - VCORE: 1 layer PWR+1 layer GND, 7 PTH Vias, S_1 length ≤ 450mil, S_1 width ≥ 150mil. (thickness ≥ 0.6mil)
      - VMODEM: 1 layer PWR+1 layer GND, 4 PTH vias, S_1 length ≤ 500mil; S_1 width ≥ 100mil. (thickness ≥ 0.6mil)
      - VSRAM
        - PROC: 1 layer PWR+1 layer GND, 1 PTH Via, S_1 length ≤ 500mil, S_1 width ≥ 30mil. (thickness ≥ 0.6mil)
        - CORE: 1 layer PWR+1 layer GND, 3 PTH Via, S1 length ≤ 500mil, S_1 width ≥ 30mil. (thickness ≥ 0.6mil)
      - VEMI_VDD2:
        - SoC: Place at least 4 0201 caps right underneath AP with 3 PTH vias.
        - DRAM: Place at least 9 0201 caps close to VEMI_VDD2 balls.
      - VEMI_VDDQ:
        - SoC: Place at least 3 0201 caps right underneath AP with 2 PTH vias.
        - DRAM: Place at least 7 0201 caps close to VEMI_VDDQ balls.
   3) S_4 is defined as the power trace segment from "bottom cap" to AP. The corresponding PCB routing rules are given as the following:
      - Place 0201 and 0402 3-terminal SMD capacitors right beneath the power balls and connect the SMD capacitors with PTH/Laser via directly to reduce mounting inductance/resistance. S_4 should be routed as short as possible.

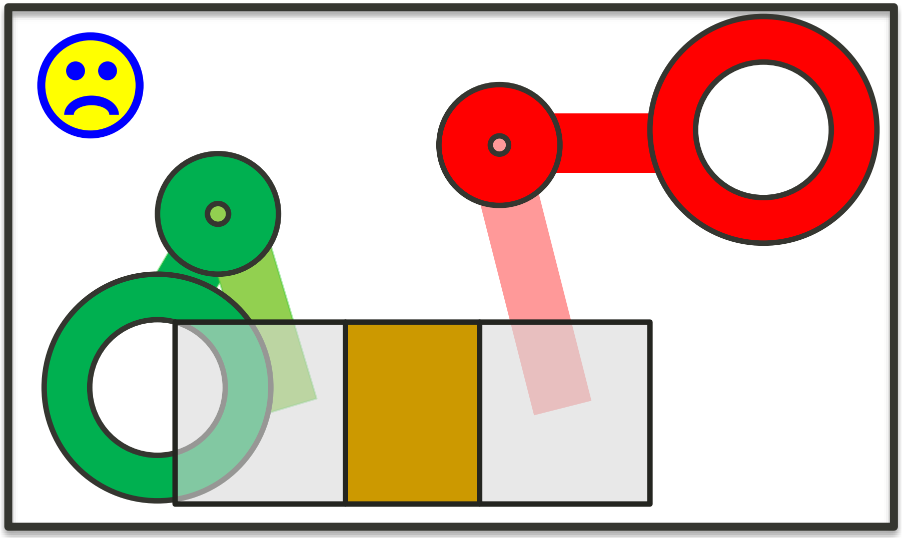
Mounting Inductance



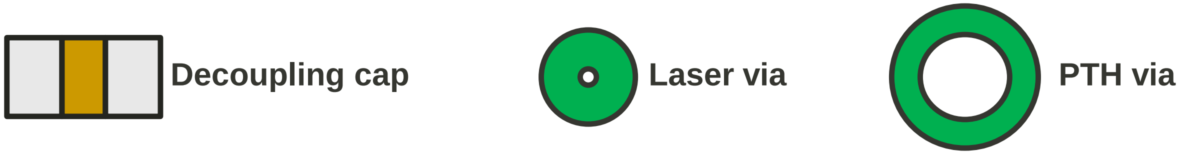
Via Interconnection



Good: Lowest mounting inductance



Bad: Excessive routing to increase inductance



Design suggestions for via interconnection

Via interconnect is critical in delivering current between each layer and is usually the bottleneck in the entire PDN networking. Thus, we strongly recommend you follow the related PWR/GND layout guidelines.

1. Connect PWR/GND via to the “wide power trace” and place it as close to the decoupling capacitor as possible.
2. Each decoupling capacitor should have at last one pair PWR/GND via. If the routing space is available, more PWR/GND vias are recommended. Try distributing PTH and Laser vias uniformly and increase PTH via as much as you can.

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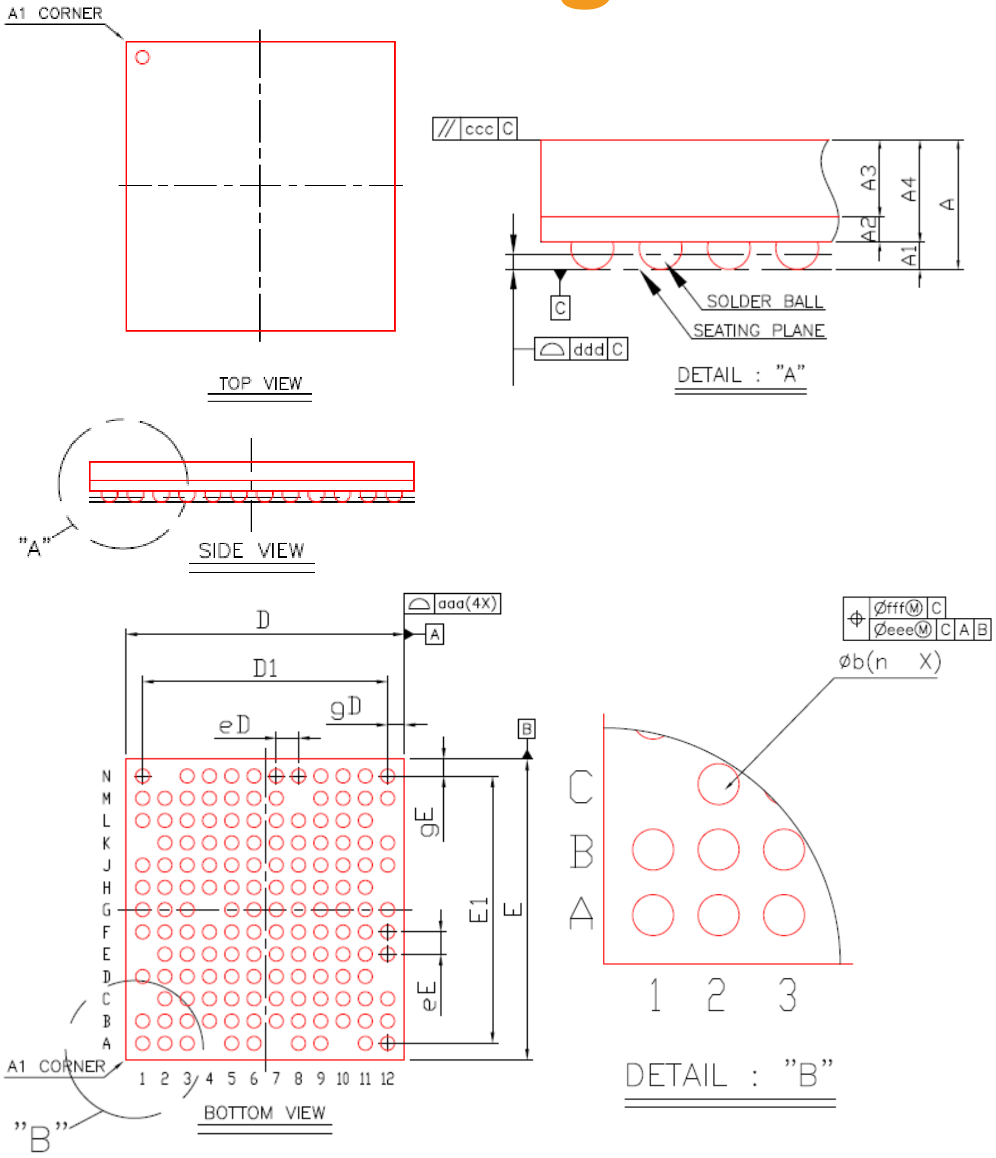
MT6177
PCB Layout Guideline

Package Outline of MT6177



Item		Symbol	Common Dimensions MIN.	NOM.	MAX.
Package Type			MFC WFBGA		
Body Size	X	D	4.90	5.00	5.10
	Y	E	5.30	5.40	5.50
Ball Pitch	X	eD	0.40		
	Y	eE	0.40		
Mold Thickness		A3	0.28 Ref.		
Substrate Thickness		A2	0.18 Ref.		
Substrate+Mold Thickness		A4	0.41	0.46	0.51
Total Thickness		A	–	–	0.70
Ball Diameter			0.25		
Ball Stand Off		A1	0.12	0.16	0.20
Ball Width		b	0.20	0.25	0.30
Package Edge Tolerance		aaa	0.05		
Mold Flatness		ccc	0.10		
Coplanarity		ddd	0.08		
Ball Offset (Package)		eee	0.15		
Ball Offset (Ball)		fff	0.05		
Ball Count		n	144		
Edge Ball Center to Center	X	D1	4.40		
	Y	E1	4.80		
Edge Ball Center to Package Edge	X	gD	0.300		
	Y	gE	0.300		

TITLE	PACKAGE OUTLINE MFC WFBGA 144L 5.0 X 5.4 X 0.7mm		MEDIATEK
DWG. NO.	REV.	SHEET	UNIT
MT-AP00502	A	1 OF 2	MM

MT6177 Ball Map

RFDRX

RFPRX

26MHz Output

LTE BSI

RF TX

LTE PRXIQ

LTE DRXIQ

LTE TXIQ

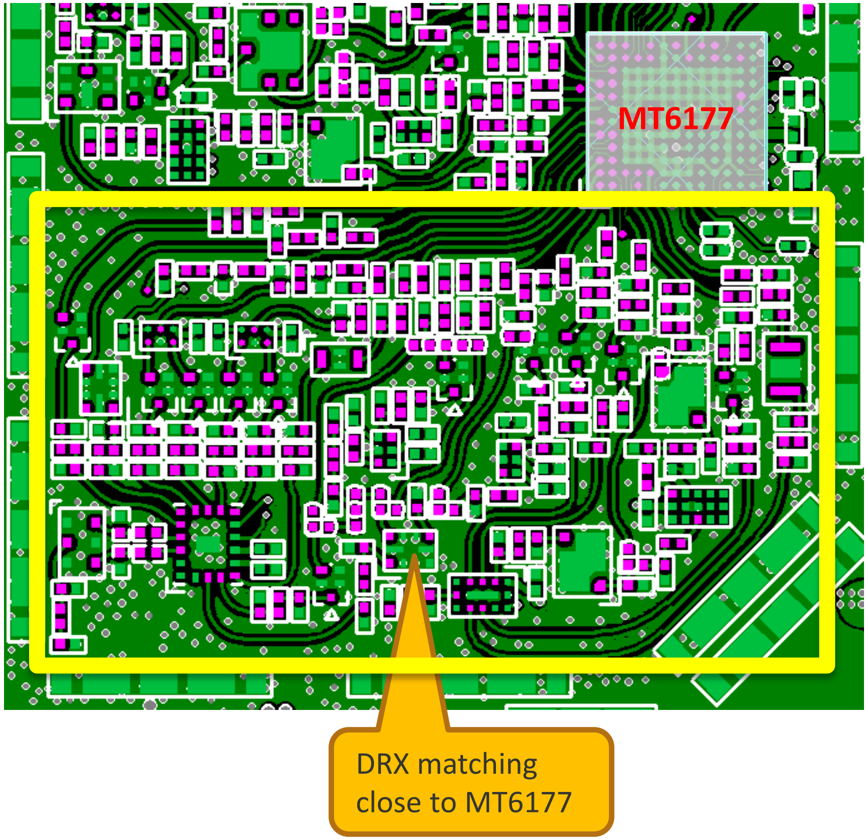
	1	2	3	4	5	6	7	8	9	10	11	12	
A	DRX10	DRX7	DRX6		DRX2	DRX1		PRX13	PRX12		PRX9	PRX8	A
B	DRX9	DRX8	DRX5	DRX4	DRX3	LAAP1	GND	PRX14	PRX11	PRX10	PRX7	PRX6	B
C		DRX11	GND	GND	GND	GND	GND	GND	GND	GND	PRX5	PRX4	C
D	DRX13	DRX12	GND	GND	GND	GND	GND	GND	GND	GND	PRX3		D
E		DRX14	GND	GND	GND	VDD_RXLV	VDD_RXHV	GND	GND	GND	PRX2	PRX1	E
F	LAAD1	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	F
G	TMEAS	GND	GND		GND	GND	GND	GND	GND	GND	TX_HB1	TX_UHB	G
H	RCAL	GND	GND	EN_BB	BSI_0_CK	GND	GND	GND	GND	GND	TX_HB2		H
J	XOI	VIO	GND	BSI_0_D0	BSI_0_EN	GND	GND	GND	GND	TXO_GND	TX_MB1	TX_MB2	J
K		GND	BSI_0_D1	BSI_0_D2	VDD_SXLV	GND	GND	GND	GND	TXO_GND	TX_LB1	TX_MB3	K
L	DRX_BB_I1	DRX_BB_Q1	GND	GND	GND	GND	GND	GND	GND	TXO_GND	TX_LB2		L
M	PRX_BB_Q1	GND	DRX_BB_Q0	PRX_BB_I0	DET_QP0	DET_IN0	TXDET1		GND	TXO_GND	TX_LB3	TX_LB4	M
N	PRX_BB_I1		DRX_BB_I0	PRX_BB_Q0	VDD_SXLF	DET_QN0	DET_IP0	VDD_TXHV	TX_BB_QN0	TX_BB_QP0	TX_BB_IN0	TX_BB_IP0	N
	1	2	3	4	5	6	7	8	9	10	11	12	

MT6177 Placement (1/3)

- RF supports PRX (Primary RX) and DRX (Diversity RX). MT6177 has two receiver circuits.
- DRX matching components should be placed near MT6177.

MT6177 DRX

IC ball number	IC ball name	PCB net name
DRX1	A6	RF_B12B17_DRX_RFIC
DRX2	A5	RF_B8_DRX_RFIC
DRX3	B5	RF_B20_DRX_RFIC
DRX4	B4	RF_B5B26B27_DRX_RFIC
DRX5	B3	RF_B28_DRX_RFIC
DRX6	A3	RF_B39_DRX_RFIC
DRX7	A2	RF_B3_DRX_RFIC
DRX8	B2	RF_B2_DRX_RFIC
DRX9	B1	RF_B32_DRX_RFIC
DRX10	A1	RF_B1B4_DRX_RFIC
DRX11	C2	RF_B40_DRX_RFIC
DRX12	D2	RF_B38B41_DRX_RFIC
DRX13	D1	RF_B7_DRX_RFIC
DRX14	E2	RF_B42_DRX_RFIC

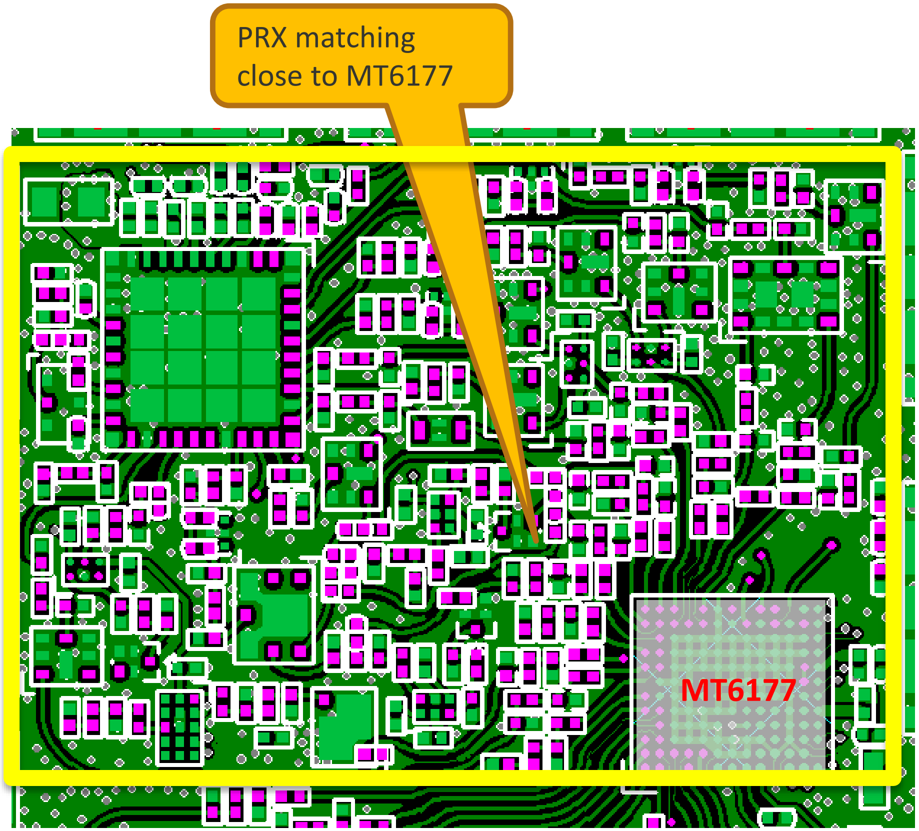


MT6177 Placement (2/3)

- PRX matching components should be placed near MT6177.

MT6177 PRX

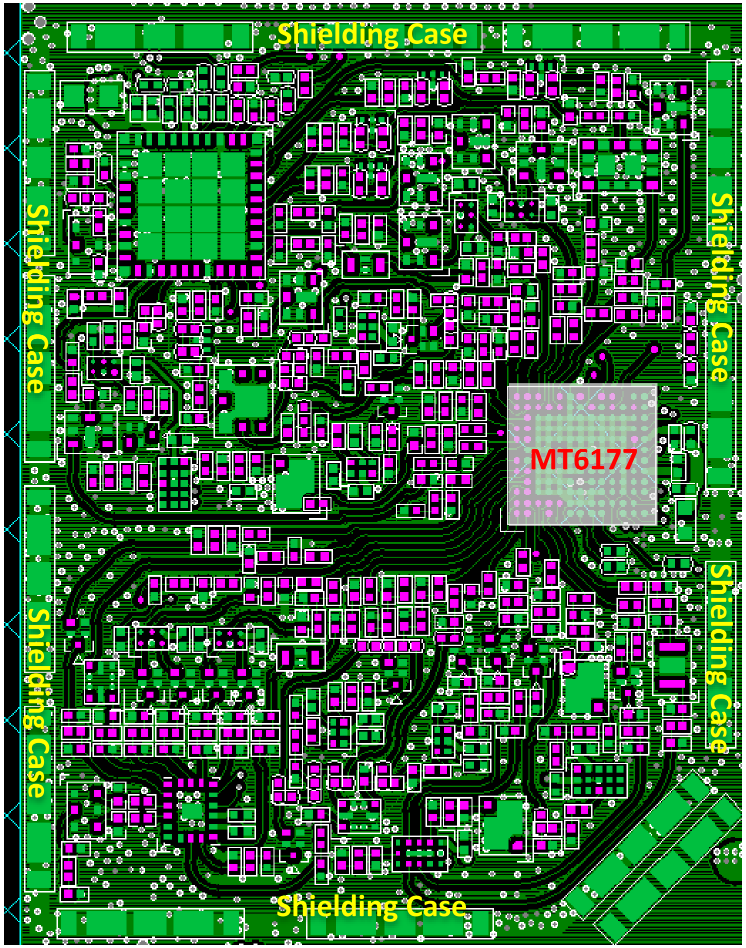
IC ball number	IC ball name	PCB net name
PRX1	E12	RF_B12B17_PRX_RFIC
PRX2	E11	RF_B8_PRX_RFIC
PRX3	D11	RF_B20_PRX_RFIC
PRX4	C12	RF_B5B26B27_PRX_RFIC
PRX5	C11	RF_B28_PRX_RFIC
PRX6	B12	RF_B34B39_PRX_RFIC
PRX7	B11	RF_B3_PRX_RFIC
PRX8	A12	RF_B2_PRX_RFIC
PRX9	A11	RF_B32_PRX_RFIC
PRX10	B10	RF_B1B4_PRX_RFIC
PRX11	B9	RF_B40_PRX_RFIC
PRX12	A9	RF_B38B41_PRX_RFIC
PRX13	A8	RF_B7_PRX_RFIC
PRX14	B8	RF_B42_PRX_RFIC



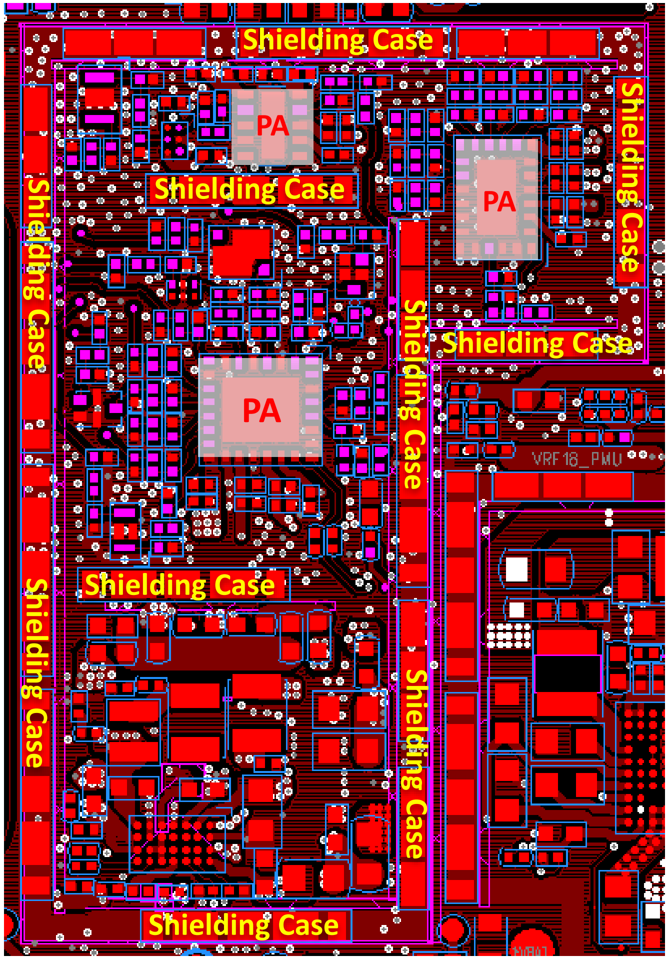
MT6177 Placement (3/3)

- MT6177 and PA IC should have their own shielding case to prevent de-sense issues.

Top side

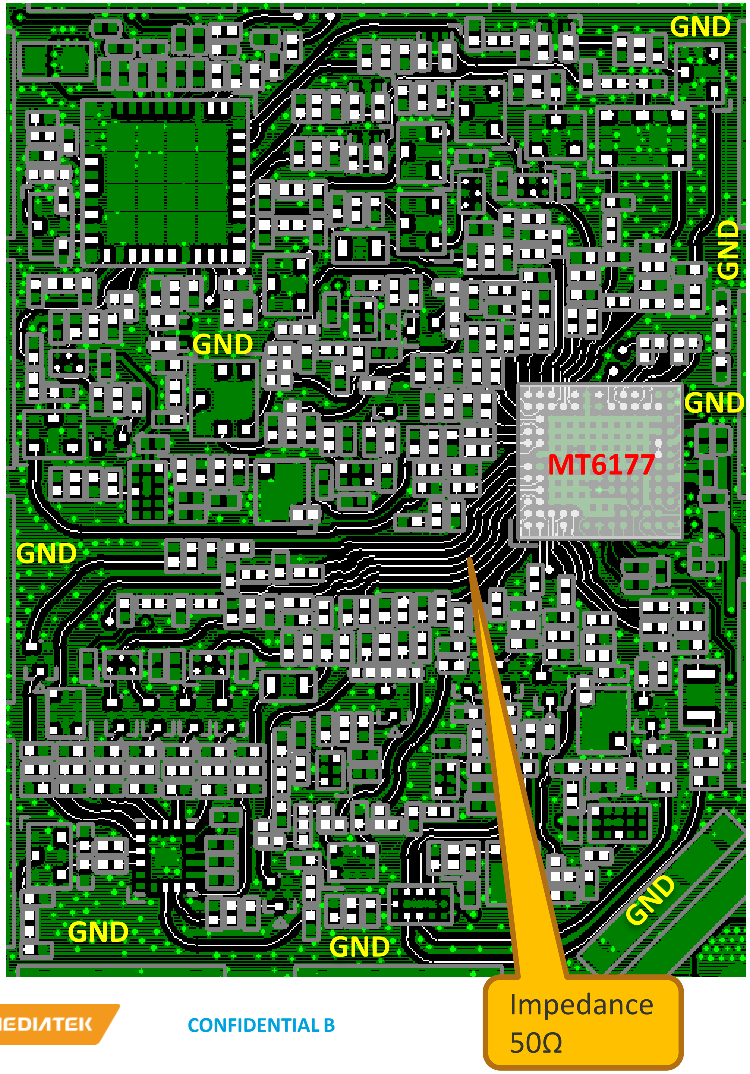


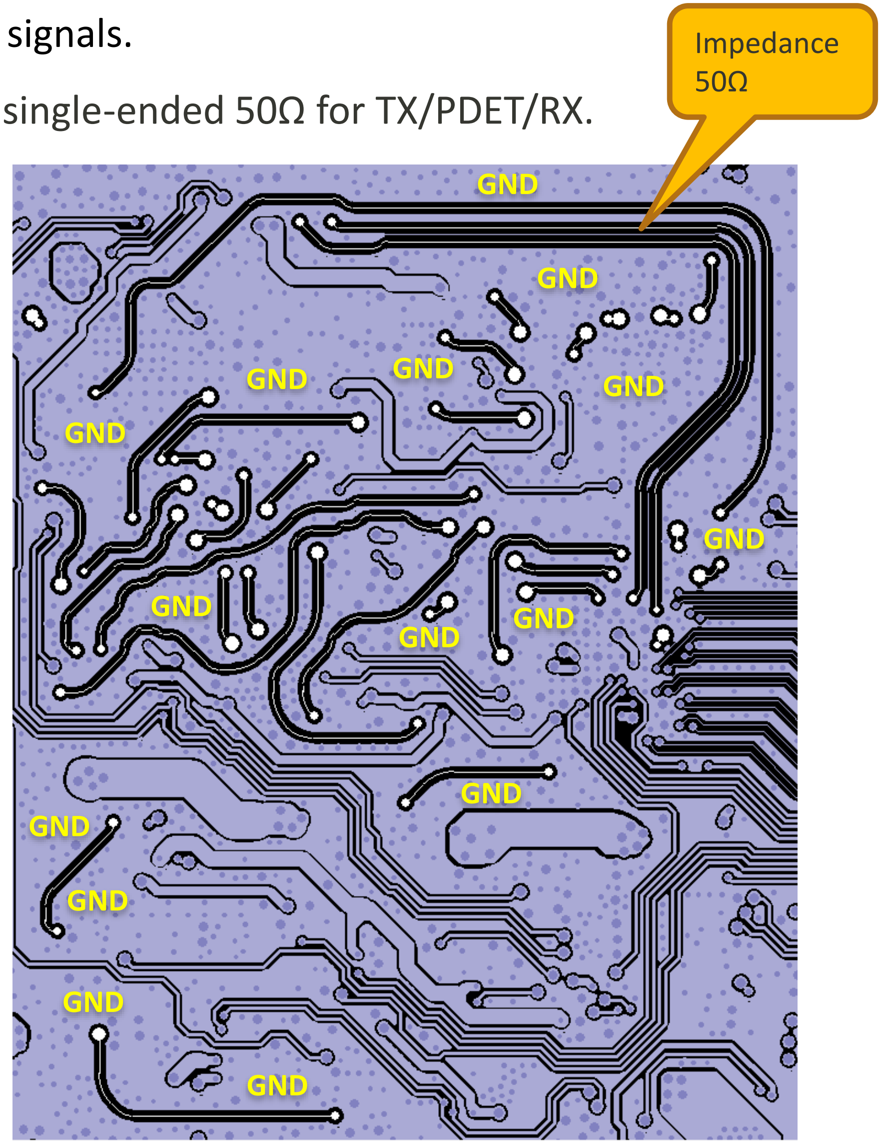
Bottom side



MT6177 TX/RX Signals

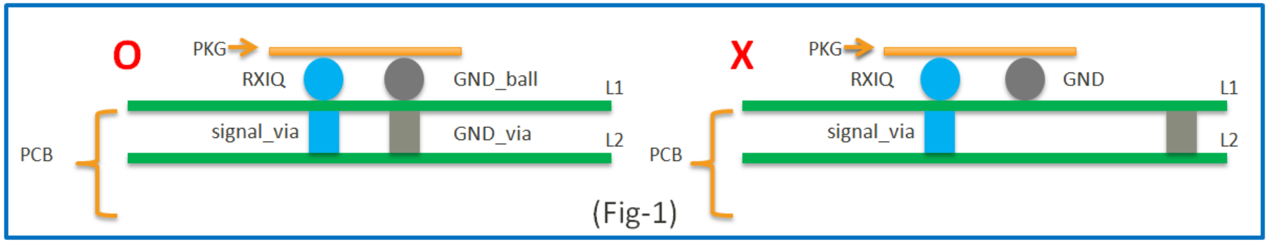
- Impedance control is necessary for all RF signals.
- Make sure that the routing impedance is single-ended 50Ω for TX/PDET/RX.



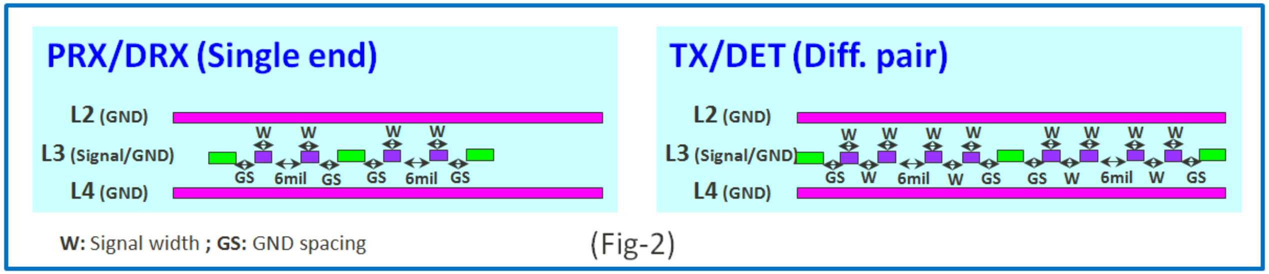


MT6177 IQ Signals (1/3)

a. All GND ball adjacent RXIQ must be well connected @ L1. (Fig-1)
b. The RXIQ signal must have GND via close to its layer transition. (Fig-1)
c. All RXIQ signals should have GND shielding by group (adjacent up/down layers). (Fig-2)
d. All TXIQ, RXIQ, DETIQ layout length must < 20mm to prevent bad isolation.



(Fig-1)



(Fig-2)

IC ball name	IC ball number
DET_IN0	M6
DET_IP0	N7
DET_QN0	N6
DET_QP0	M5
DRX_BB_I0	N3
DRX_BB_I1	L1
DRX_BB_Q0	M3
DRX_BB_Q1	L2
PRX_BB_I0	M4
PRX_BB_I1	N1
PRX_BB_Q0	N4
PRX_BB_Q1	M1
TX_BB_IN0	N11
TX_BB_IP0	N12
TX_BB_QN0	N9
TX_BB_QP0	N10

MT6177 IQ

MT6177 IQ Signals (2/3)

Layout not recommended
Figure 1 shows the ABB IQ are routed beneath the PMIC power nets even with ground plane shielding; however, the magnetic coupling from PMIC switching node can cause de-sense issues.

Layout recommended
Figure 2 shows the ABB IQ are routed away from PMIC power nets to avoid de-sense issue. No overlap between PMIC nets and ABB IQ region.

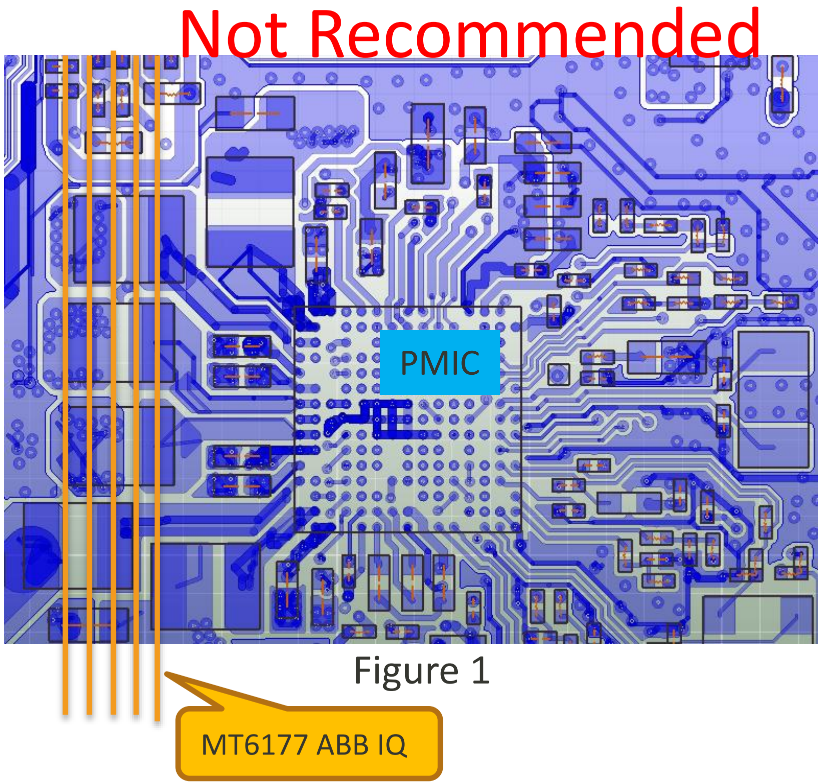


Figure 1

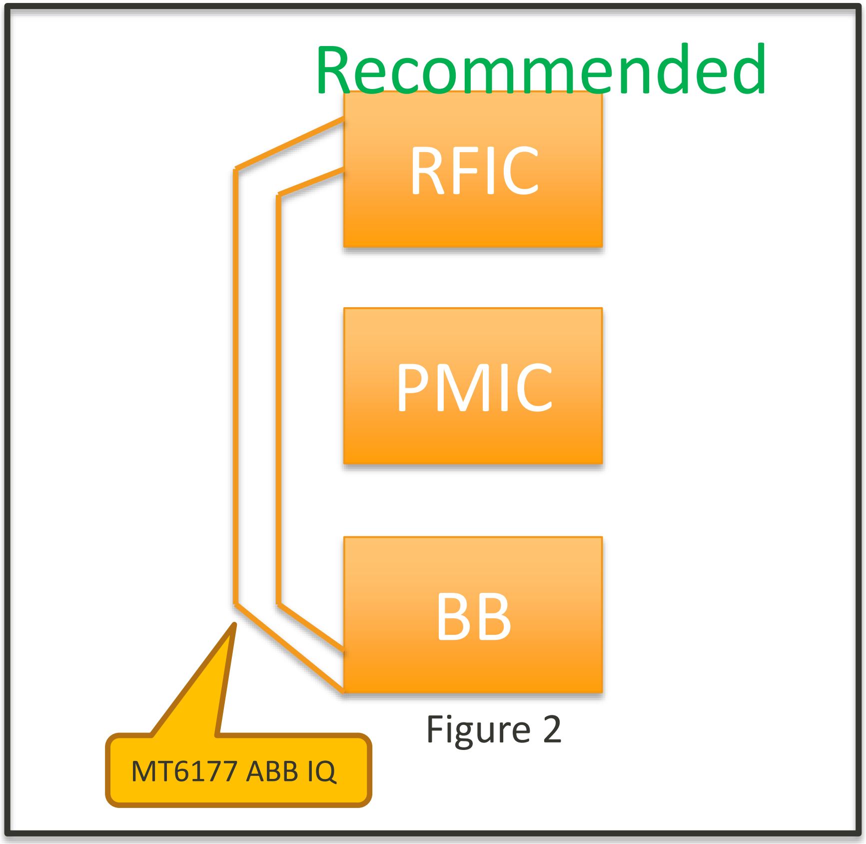


Figure 2

MT6177 IQ Signals (3/3)

Layout not recommended
Figure 1 shows the PMIC power nets via are routed in the ABB IQ region in the PCB inner layer even with ground shielding; however, the low frequency PMIC switching noise can couple to RX IQ and cause de-sense issues.

Layout recommended
Figure 2 shows PMIC power nets via are away from ABB IQ region at least 25mil to avoid de-sense issues.

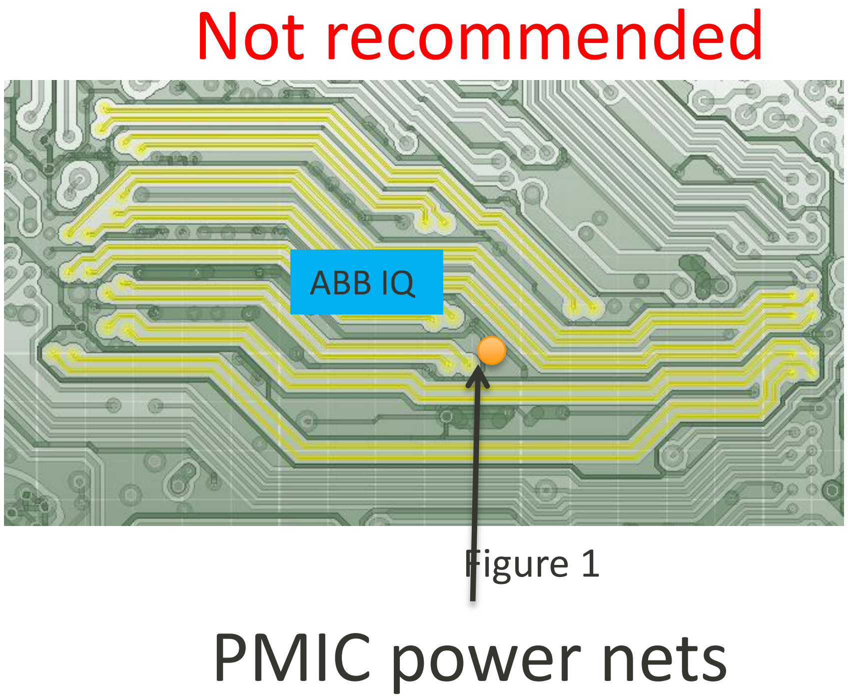


Figure 1

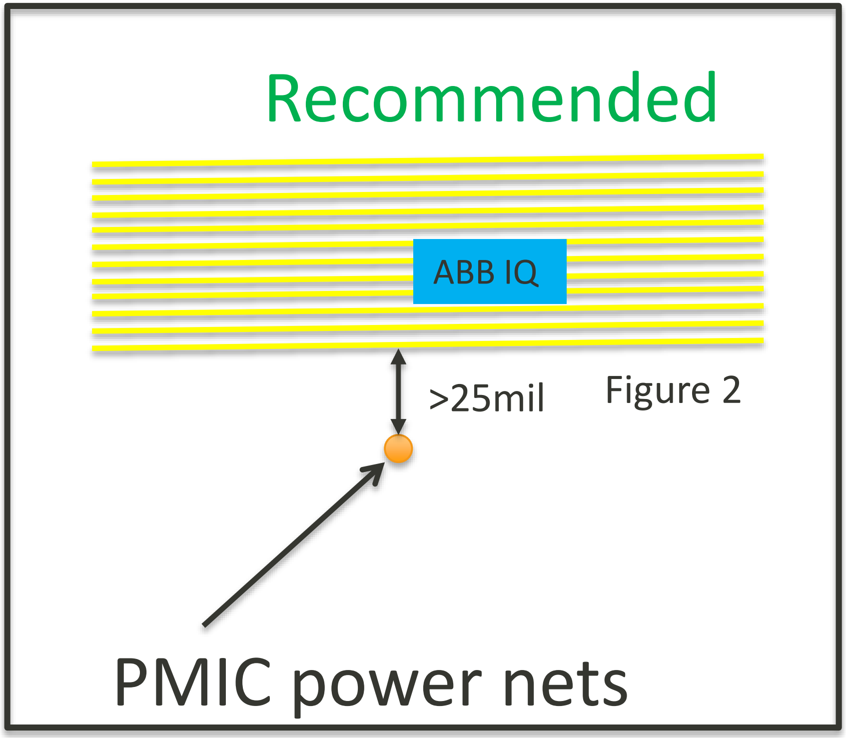
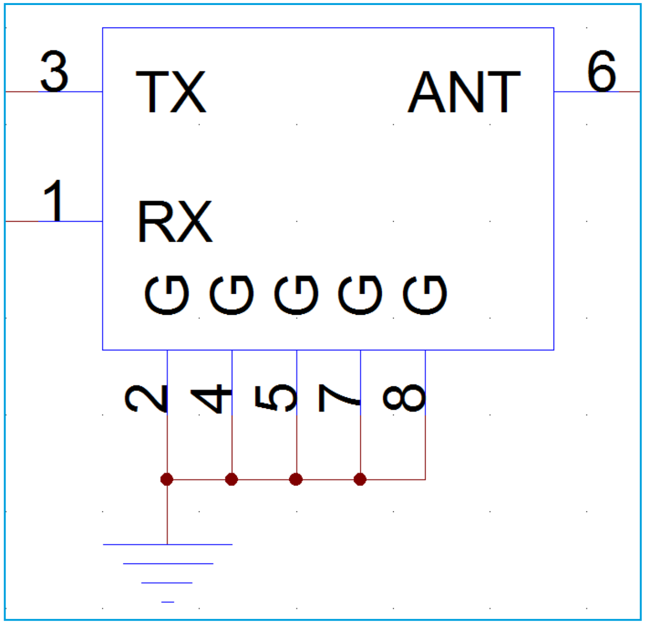


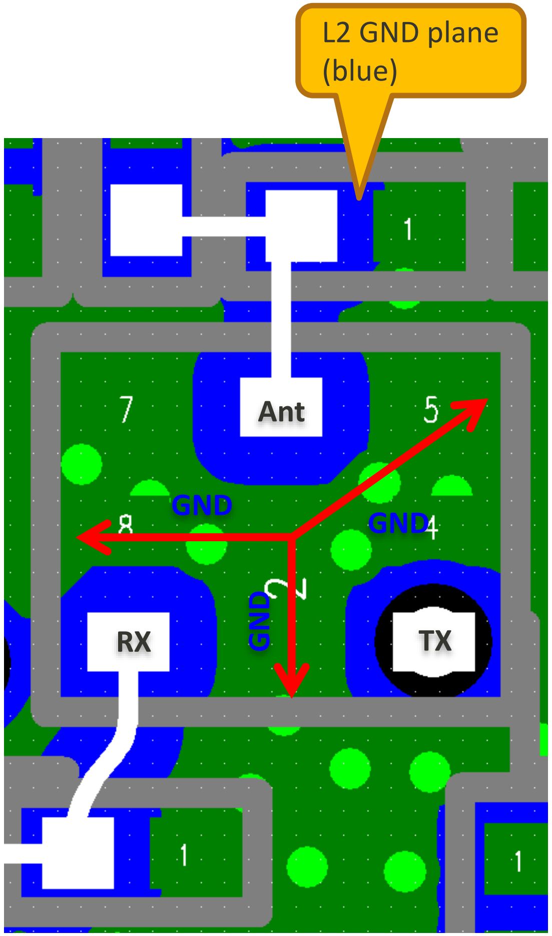
Figure 2

MT6177 Duplexer

- **Duplexer notice**

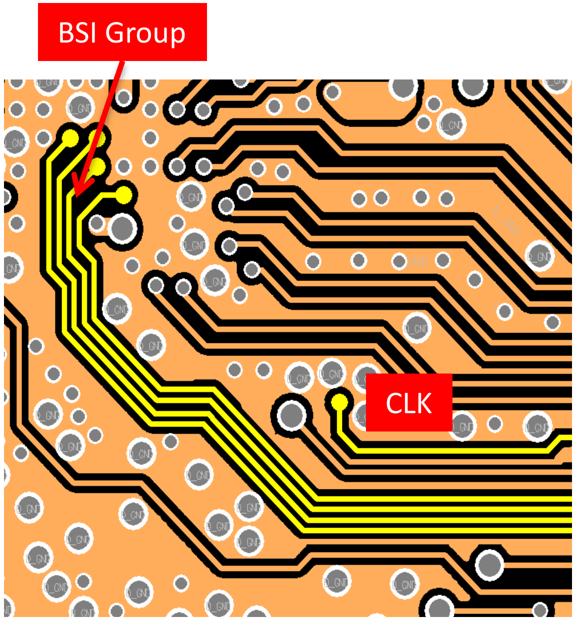
a. Enlarge L1 copper pouring range for duplexer GND pins (2, 4, 5, 7, 8).
b. Avoid parallel routing between ANT/RX/TX signals.
c. Maintain good isolation between ANT/RX/TX by:
   1. GND shielding between these three paths.
   2. Good grounding with plenty of GND via.
d. There should be good GND plane at L2 for reference.





Others for MT6177

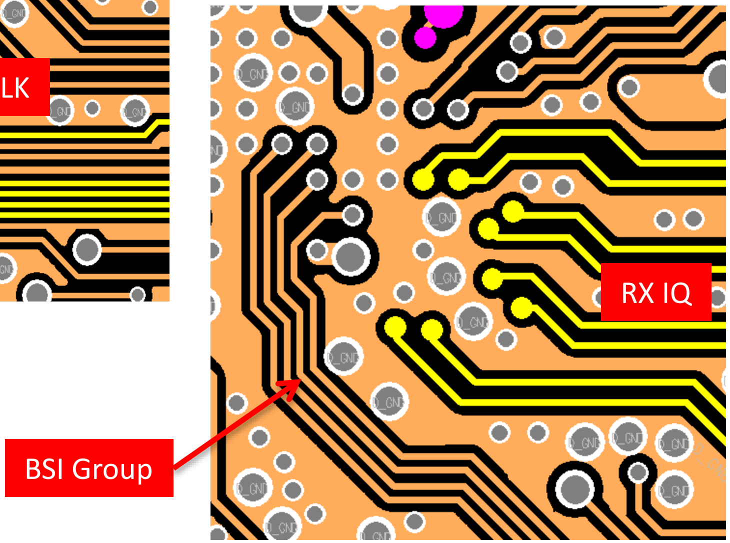
a. CLK signal should have GND shielding and avoid routing this net between BSI signals. (Fig-1)
b. BSI signals should have GND shielding by group (adjacent up/down layers). (Fig-1)
c. Must have ground via close to the RXIQ when layer change happens. (Fig-2)
d. RFFE MIPI signal (MIPI0_SCLK, MIPI0_SDATA) should be as far as possible from RF signals. (Fig-3)



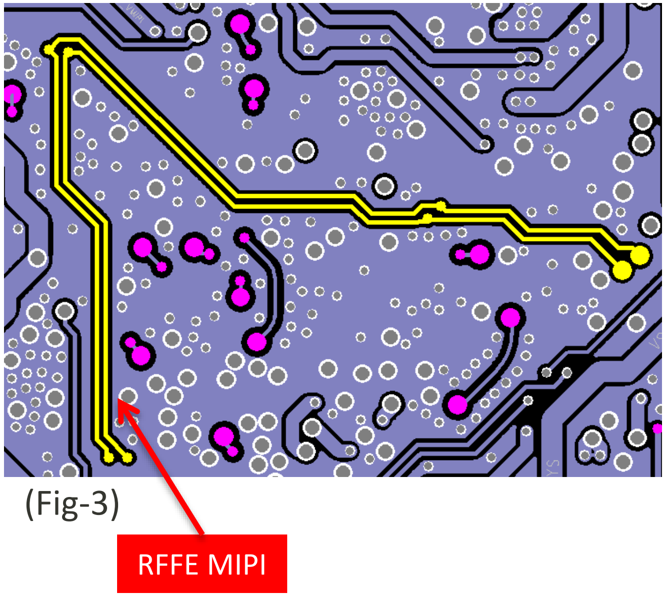
(Fig-1)

MT6177 BSI

IC ball name	IC ball number
BSI_0_CK	H5
BSI_0_D0	J4
BSI_0_D1	K3
BSI_0_EN	J5



(Fig-2)



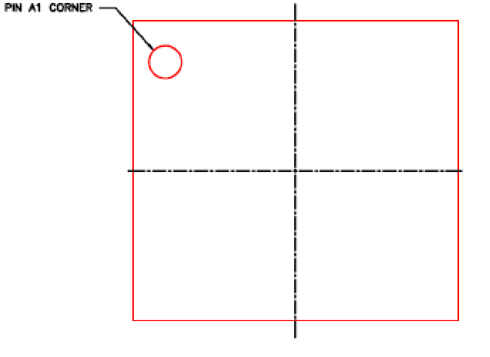
(Fig-3)

Outlines

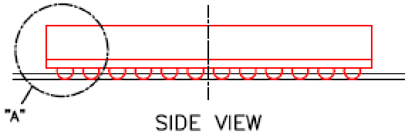
- **Packaging**
  - Package outline of MT6765
  - MT6765 footprint recommendation
  - MT6765 ball out design
- **General Guidelines**
  - PCB stack-up recommendation
  - Placement notes
- **Design Guidelines for High-speed Digital Signals**
  - LPDDR4X/LPDDR3
  - PDN design
- **Others**
  - MT6765 RF interface - MT6177 (RF transceiver)
  - MT6765 RF interface - MT6177M (RF transceiver)
  - MT6631 (BT/FM/Wi-Fi/GPS)
  - MT6371 (battery charger/USB_PD)
  - eMMC/USB/MIPI/SIM card/T-card

MT6177M
PCB Layout Guideline

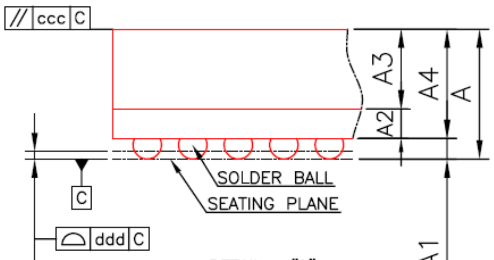
Package Outline of MT6177M



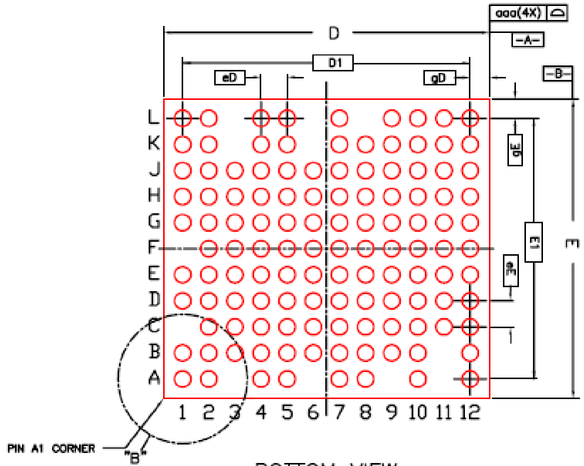
TOP VIEW



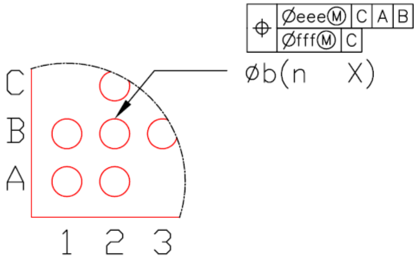
SIDE VIEW



DETAIL : "A"



BOTTOM VIEW



DETAIL : "B"

Item		Symbol	Common Dimensions		
			MIN.	NOM.	MAX.
Package Type			VFBGA		
Body Size	X	D	4.9	5.0	5.1
	Y	E	4.5	4.6	4.7
Ball Pitch	X	eD	0.40		
	Y	eE	0.40		
Mold Thickness		A3	0.53 Ref.		
Substrate Thickness		A2	0.13 Ref.		
Substrate+Mold Thickness		A4	0.61	0.66	0.71
Total Thickness		A	–	–	0.90
Ball Diameter			0.25		
Ball Stand Off		A1	0.12	0.16	0.20
Ball Width		b	0.20	0.25	0.30
Package Edge Tolerance		aaa	0.05		
Mold Flatness		ccc	0.10		
Coplanarity		ddd	0.08		
Ball Offset (Package)		eee	0.15		
Ball Offset (Ball)		fff	0.05		
Ball Count		n	120		
Edge Ball Center to Center	X	D1	4.40		
	Y	E1	4.00		
Edge Ball Center to Package Edge	X	gD	0.30		
	Y	gE	0.30		

TITLE	PACKAGE OUTLINE VFBGA 120 L 5.0 X4.6 X0.90mm		
DWG. NO.	REV.	SHEET	UNIT
MT-P00532	A	1 OF 2	MM

MT6177M Ball Map

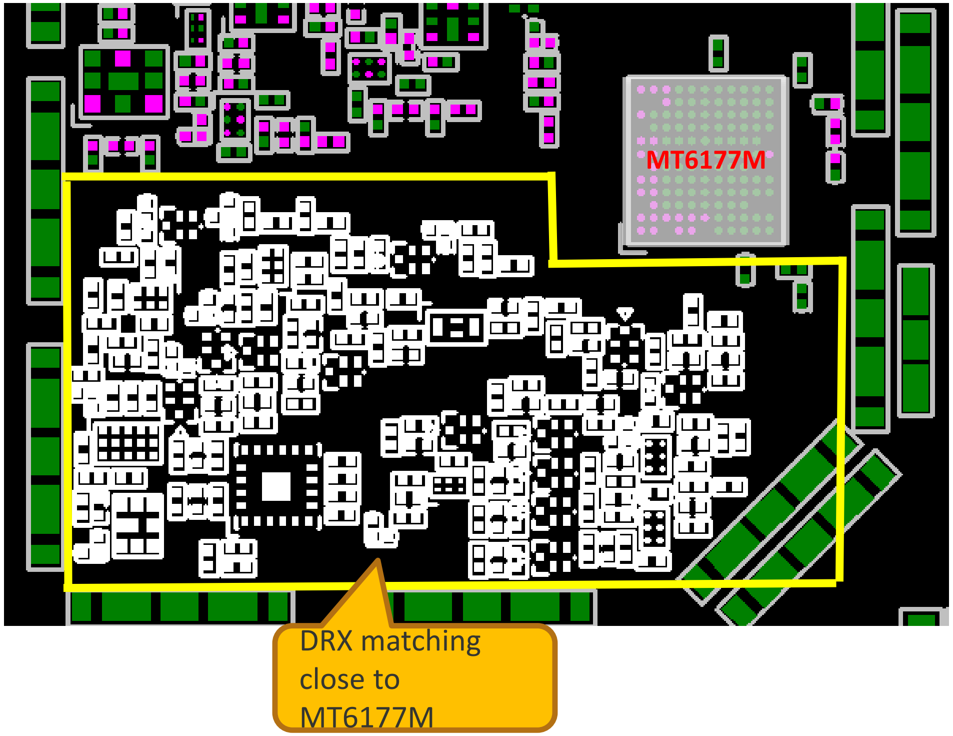
	1	2	3	4	5	6	7	8	9	10	11	12			
A	DRX2	DRX1		PRX8	PRX6		PRX4	PRX2		TXO4(2G)		TXO3(2G)	A		RF_DRx
B	DRX4	DRX3	SWLB	SWHB	PRX7	PRX5	PRX3	PRX1	GND	TX_GND		TX_GND	B		RF_PRx
C		DRX5	GND	GND	GND	GND	GND	GND	GND	TX_GND	TXO5	TXO2	C		RF_Tx
D	DRX6	DRX7	GND	GND	GND	GND	GND	GND	GND	TX_GND	TX_GND	TXO1	D		power
E	DRX8	DRX9	VDD_RXLV	GND	GND	GND	GND	GND	GND	GND	GND	GND	E		BSI
F		DRX10	GND	GND	GND	GND	GND	GND	GND	STX_MON	GND	VDD_TXHF	F		TX_IQ
G	RCAL	VDD_RXHF	GND	EN_BB	GND	GND	GND	GND	GND	GND	GND	GND	G		DET_IQ
H	BSI_EN	BSI_D0	GND	GND	GND	GND	GND	GND	GND	GND	GND	TX_BBIP	H		PRX_IQ
J	BSI_D1	BSI_D2	RX2_BBIP	RX2_BBIN	RX1_BBQN	RX1_BBQP	GND	GND	GND	VDD_STXHF	GND	TX_BBIN	J		DRX_IQ
K	BSI_CLK	GND		RX2_BBQN	RX1_BBIN		DET_QP	DET_QN	DET_IN	GND	GND	TX_BBQN	K		XO_IN
L	VIO	XO_IN		RX2_BBQP	RX1_BBIP		TXDET1		DET_IP	GND	VDD_STXLV	TX_BBQP	L		TX_DET
	1	2	3	4	5	6	7	8	9	10	11	12			GND

MT6177M Placement (1/3)

- RF supports PRX (Primary RX) and DRX (Diversity RX).
- DRX matching components should be placed near MT6177M as the figure below.

MT6177M DRX

IC ball number	IC ball name	PCB net name
DRX1	A2	RF_B1_DRX_RFIC
DRX2	A1	RF_B2_DRX_RFIC
DRX3	B2	RF_B41_DRX_RFIC
DRX4	B1	RF_B3_DRX_RFIC
DRX5	C2	RF_B7_DRX_RFIC
DRX6	D1	RF_B40_DRX_RFIC
DRX7	D2	RF_B39_DRX_RFIC
DRX8	E1	RF_B26_DRX_RFIC
DRX9	E2	RF_B8B20_DRX_RFIC
DRX10	F2	RF_B28BB12_DRX_RFIC

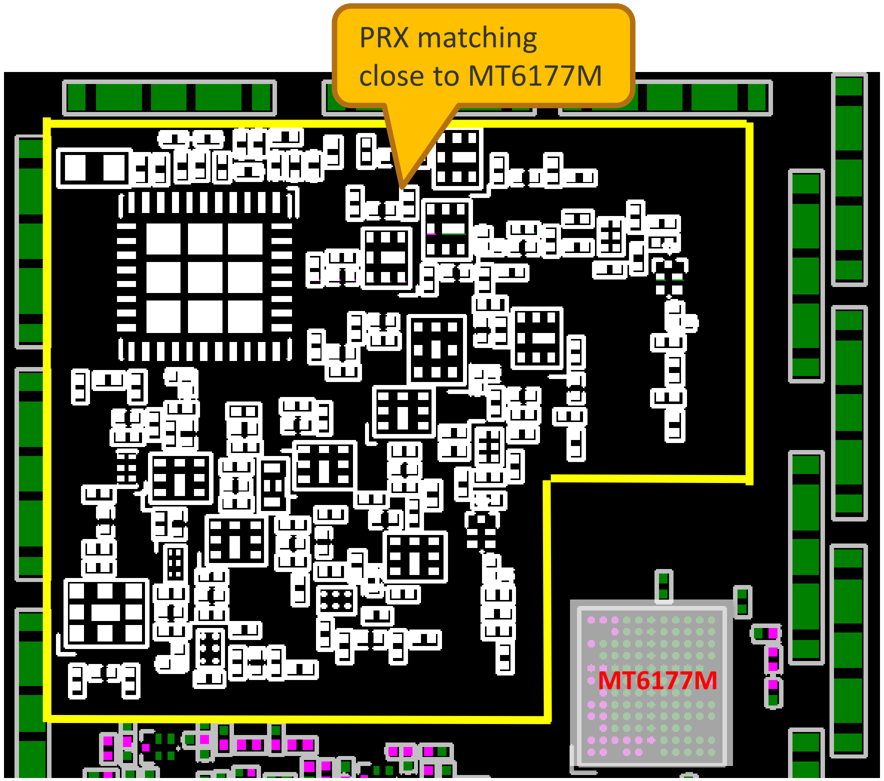


MT6177M Placement (2/3)

- PRX matching components should be placed near MT6177M.

MT6177M PRX

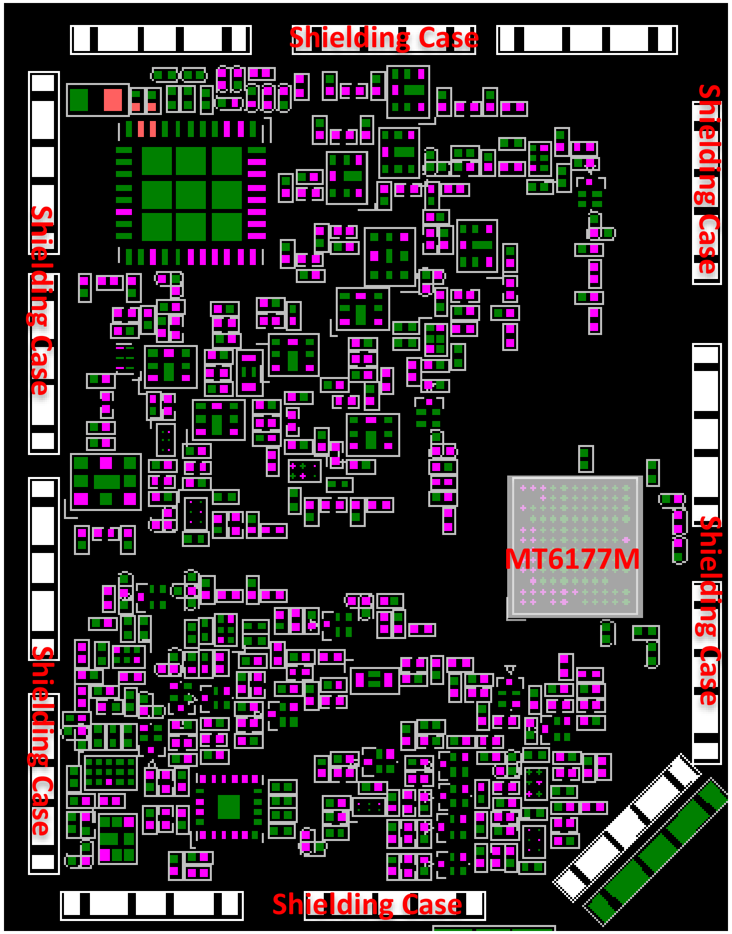
IC ball number	IC ball name	PCB net name
PRX1	B8	RF_B3_PRX_RFIC
PRX2	A8	RF_B1_PRX_RFIC
PRX3	B7	RF_B4_PRX_RFIC
PRX4	A7	RF_B40B41_PRX_RFIC
PRX5	B6	RF_B26_PRX_RFIC
PRX6	A5	RF_B7_PRX_RFIC
PRX7	B5	RF_B2_PRX_RFIC
PRX8	A4	RF_B12B28B_PRX_RFIC
SWHB	B4	RF_B34B39_PRX_RFIC
SWLB	B3	RF_B8B20_PRX_RFIC



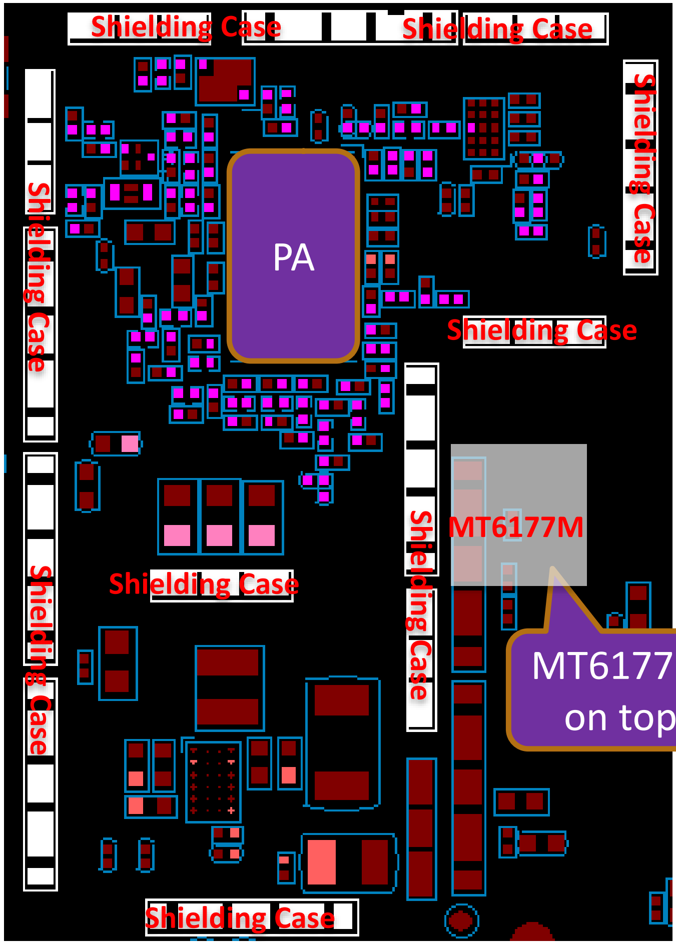
MT6177M Placement (3/3)

- MT6177M and PA IC should have their own shielding case to prevent de-sense issues.

Top side

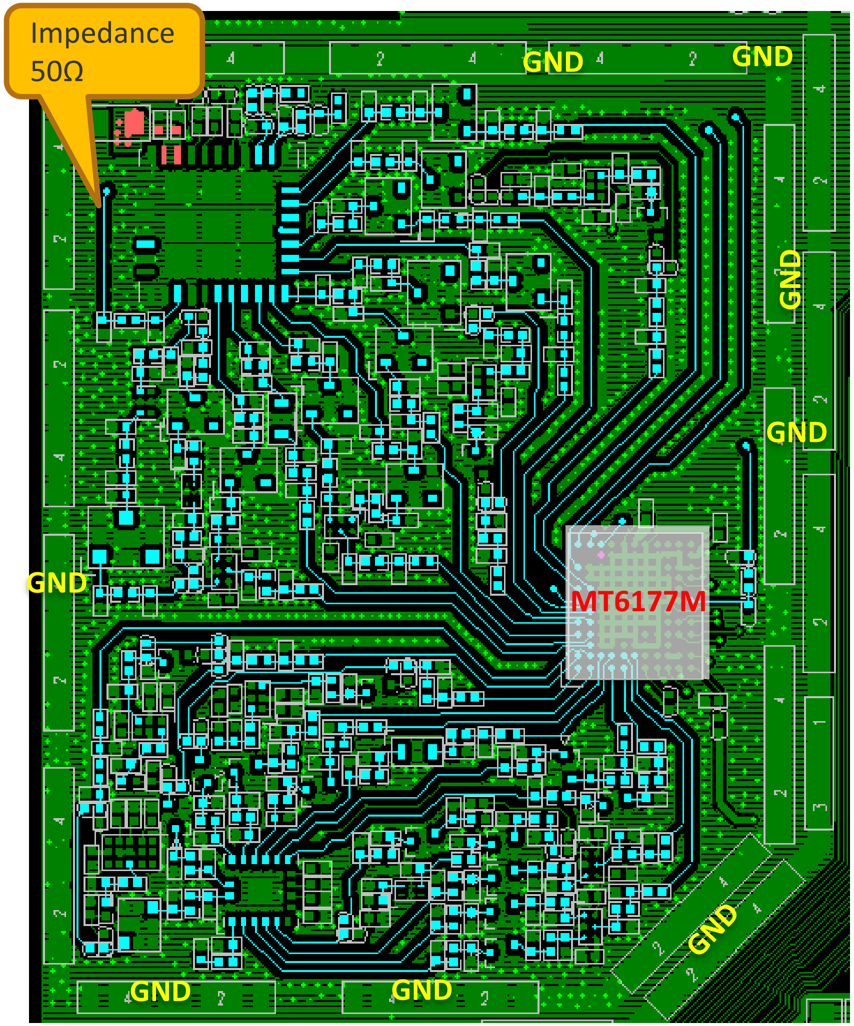


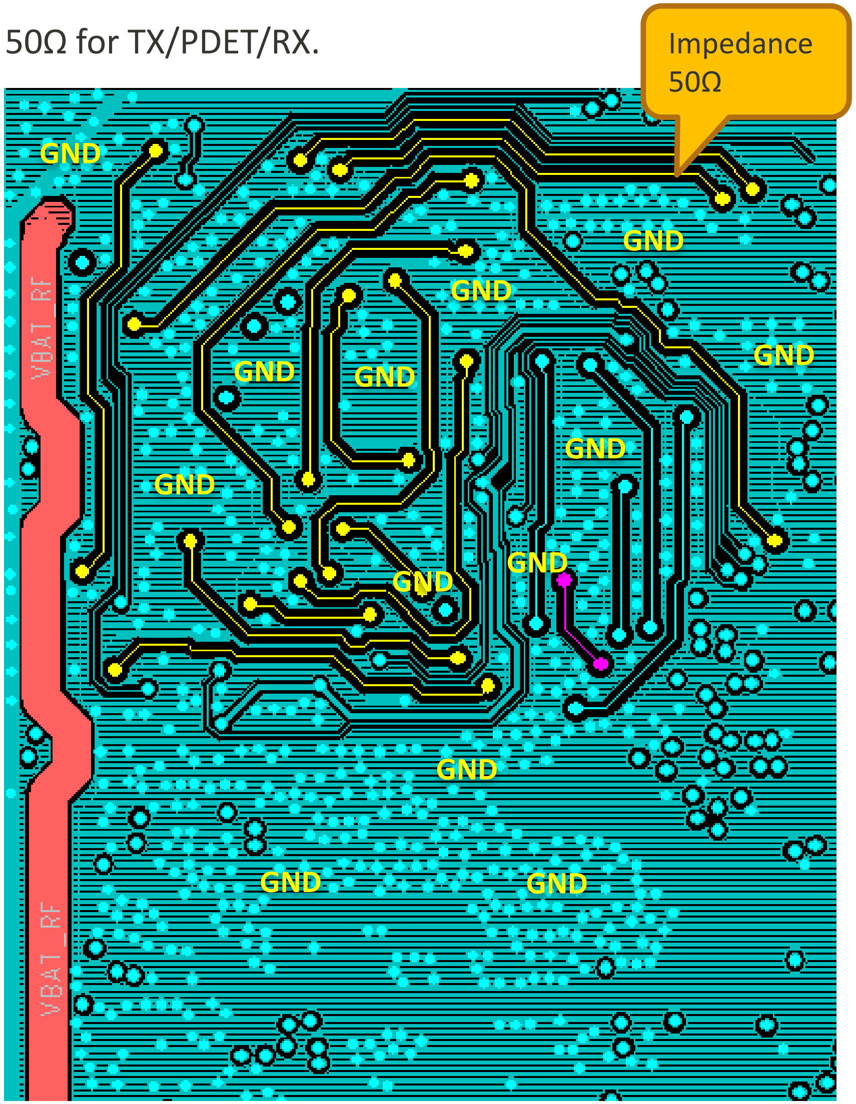
Bottom side



MT6177M TX/RX Signals

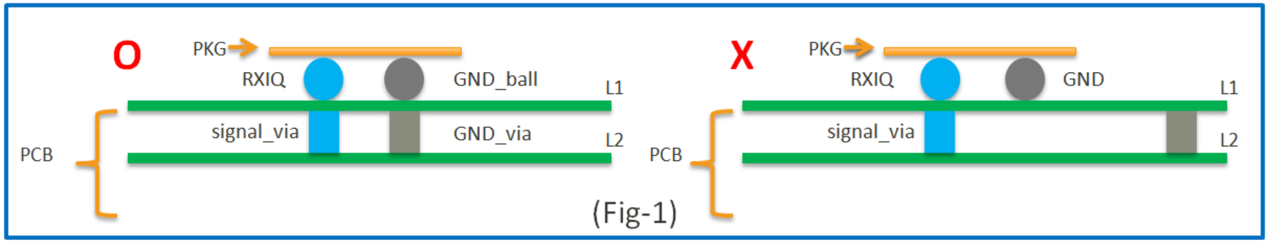
- Impedance control is necessary for all RF signals.
- Make sure that the routing impedance is single-ended 50Ω for TX/PDET/RX.



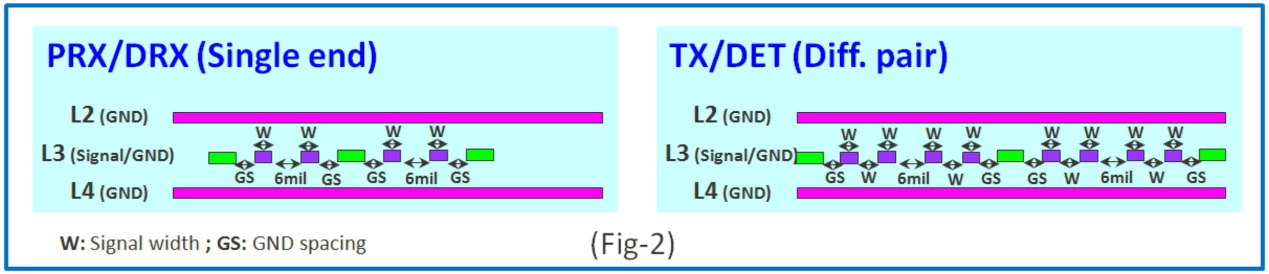


MT6177M IQ Signals

a. All GND ball adjacent RXIQ must be well connected @ L1. (Fig-1)
b. The RXIQ signal must have GND via close to its layer transition. (Fig-1)
c. All RXIQ signals should have GND shielding by group (adjacent up/down layers). (Fig-2)
d. All TXIQ, RXIQ, DETIQ layout length must < 20mm to prevent bad isolation.



(Fig-1)



(Fig-2)

IC ball name	IC ball number
RX2_BBIP	J3
RX2_BBIN	J4
RX2_BBQP	L4
RX2_BBQN	K4
RX1_BBIP	L5
RX1_BBIN	K5
RX1_BBQP	J6
RX1_BBQN	J5
TX_BBIP	H12
TX_BBIN	J12
TX_BBQP	L12
TX_BBQN	K12
DET_IP	L9
DET_IN	K9
DET_QP	K7
DET_QN	K8

MT6177M IQ

MT6177M Duplexer

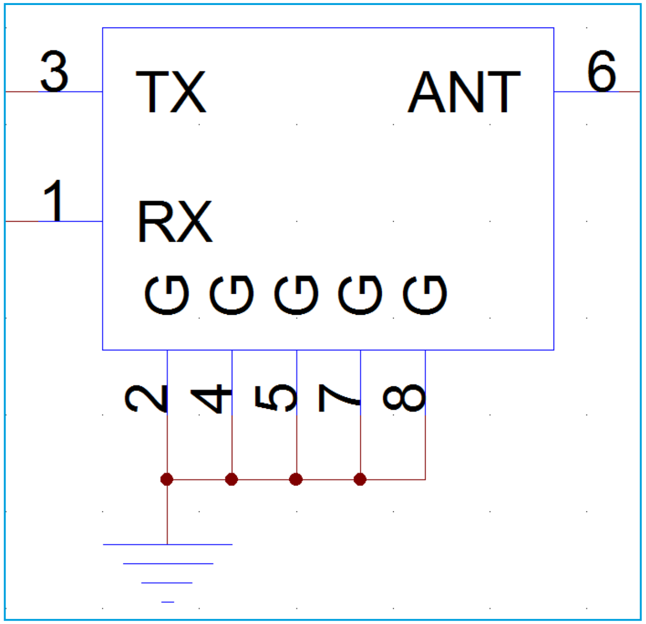
- **Duplexer notice**

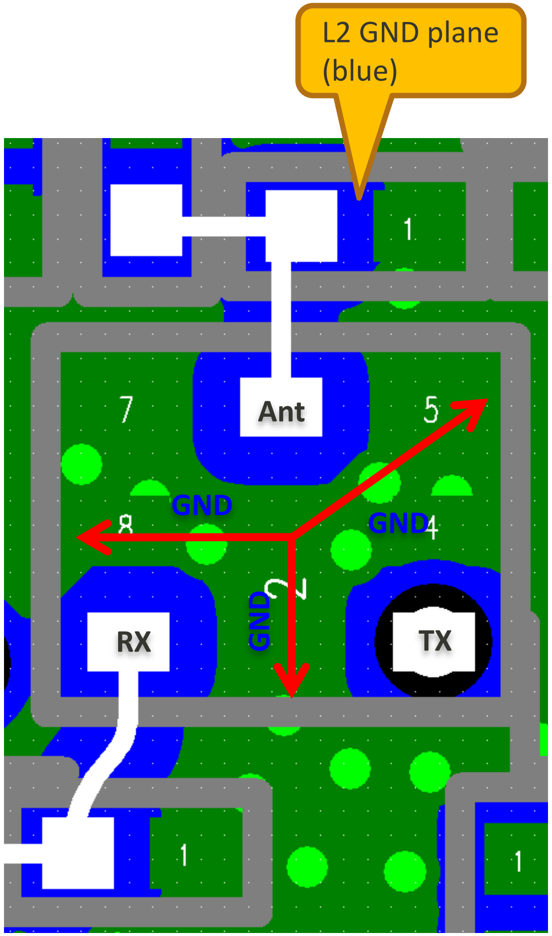
a. Enlarge L1 copper pouring range for duplexer GND pins (2, 4, 5, 7, 8).

b. Avoid parallel routing between ANT/RX/TX signals.

c. Maintain good isolation between ANT/RX/TX by:
   1. GND shielding between these three paths
   2. Good grounding with plenty of GND via

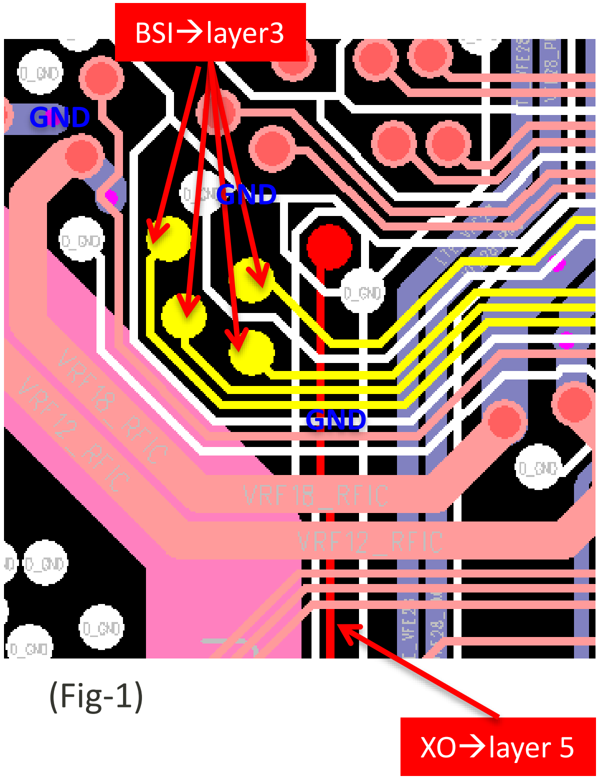
d. There should be good GND plane at L2 for reference.





Others for MT6177M

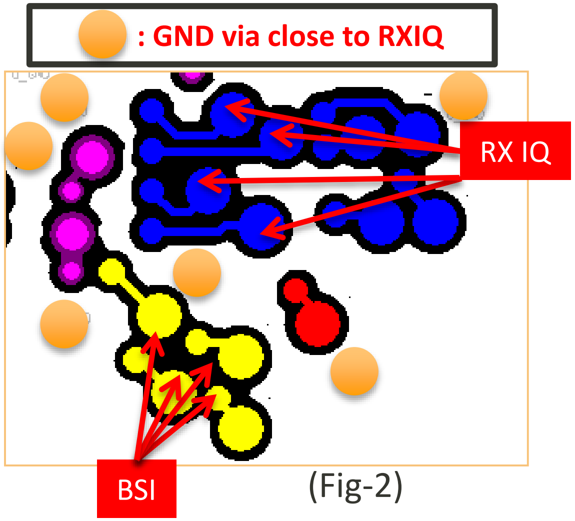
a. XO signal should have GND shielding and avoid routing this net between BSI signals. Routing them in different layer is better. (Fig-1)
b. BSI signals should have GND shielding by group (adjacent up/down layers). (Fig-1)
c. Must have ground via close to the RXIQ when layer change happens. (Fig-2)
d. RFFE MIPI signal (MIPI0_SCLK , MIPI0_SDATA) should be as far as possible from RF signals. (Fig-3)



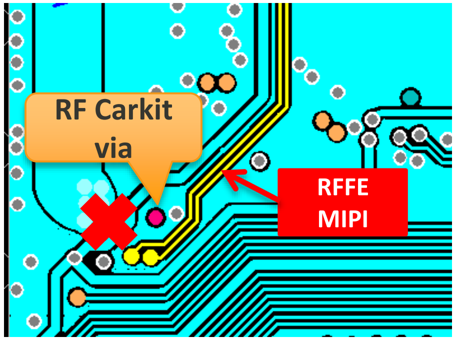
(Fig-1)

MT6177M BSI

IC ball name	IC ball number
BSI_CLK	K1
BSI_D0	H2
BSI_D1	J1
BSI_D2	J2
BSI_EN	H1



(Fig-2)



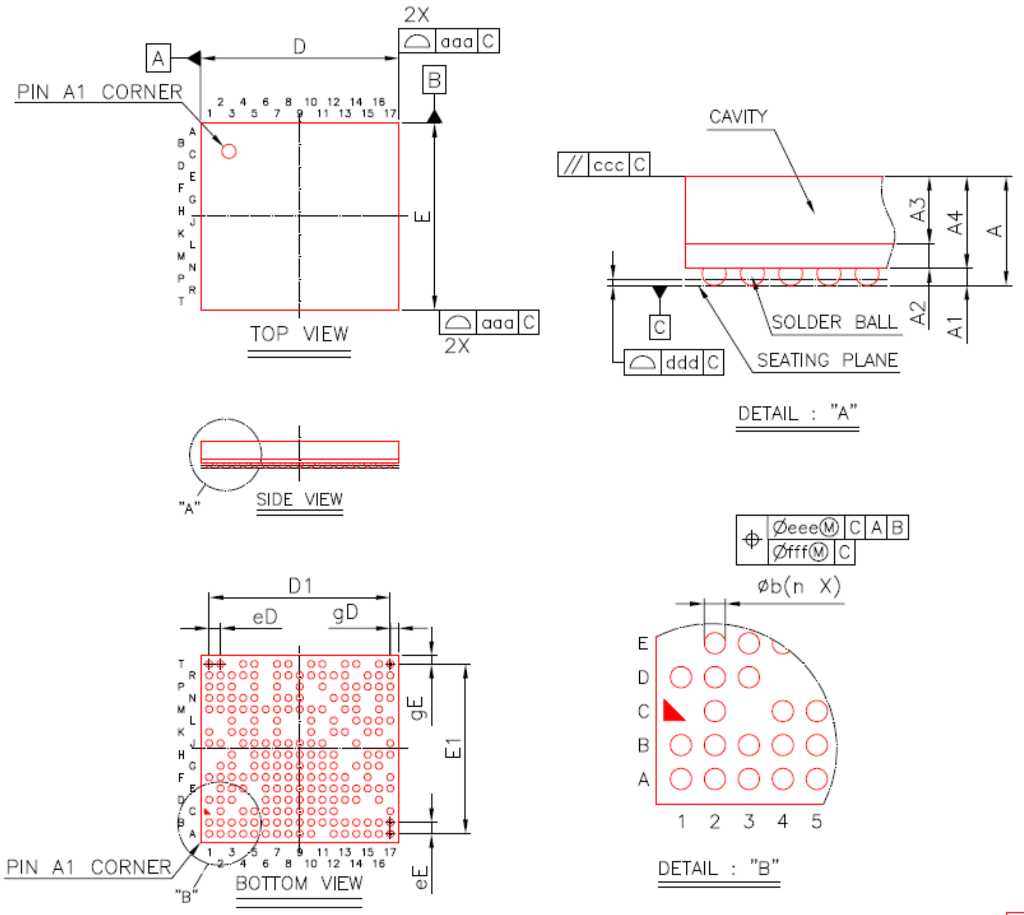
(Fig-3)

Outlines

- **Packaging**
  - Package outline of MT6765
  - MT6765 footprint recommendation
  - MT6765 ball out design
- **General Guidelines**
  - PCB stack-up recommendation
  - Placement notes
- **Design Guidelines for High-speed Digital Signals**
  - LPDDR4X/LPDDR3
  - PDN design
- **Others**
  - MT6765 RF interface - MT6177 (RF transceiver)
  - MT6765 RF interface - MT6177M (RF transceiver)
  - MT6357 (PMU)
  - MT6631 (BT/FM/Wi-Fi/GPS)
  - MT6371 (battery charger/USB_PD)
  - eMMC/USB/MIPI/SIM card/T-card

MT6357
PCB Layout Guideline

Package Outline of MT6357



Item		Symbol	Common Dimensions MIN.	NOM.	MAX.
Package Type				VFBGA	
Body Size	X	D	6.90	7.00	7.10
	Y	E	6.50	6.60	6.70
Ball Pitch	X	eD		0.40	
	Y	eE		0.40	
Mold Thickness		A3		0.65 Ref.	
Substrate Thickness		A2		0.13 Ref.	
Substrate+Mold Thickness		A4	0.73	0.78	0.83
Total Thickness		A	–	–	1.00
Ball Diameter				0.25	
Ball Stand Off		A1	0.12	0.16	0.20
Ball Width		b	0.20	0.25	0.30
Package Edge Tolerance		aaa		0.05	
Mold Flatness		ccc		0.10	
Coplanarity		ddd		0.08	
Ball Offset (Package)		eee		0.15	
Ball Offset (Ball)		fff		0.05	
Ball Count		n		209	
Edge Ball Center to Center	X	D1		6.40	
	Y	E1		6.00	
Edge Ball Center to Package Edge	X	gD		0.30	
	Y	gE		0.30	

TITLE	PACKAGE OUTLINE VFBGA 209L 7.0X6.6 X 1.0mm		MEDIATEK	
	DWG. NO.	REV.	SHEET	UNIT
	MT-P00570	A	1 OF 2	MM

MT6357 Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
A	VPA	VSYS_VPA	VSYS_VPA	VSYS_VPROC	GND_VPROC	VPROC	VPROC	VSYS_VCORE	VCORE	VCORE		GND_VMODEM	VSYS_VMODEM	VSYS_VS1	GND_VS1	VS1	VCAMIO	A
B	GND_SMPS	VSYS_SMPS	GND_VPA	VSYS_VPROC	GND_VPROC	VPROC	VPROC	VSYS_VCORE	GND_VCORE	VCORE	VMODEM	GND_VMODEM	VSYS_VMODEM	VSYS_VS1	GND_VS1	VS1	VIO18	B
C		VPROC_FB		VSYS_VPROC	GND_VPROC	VPROC	VPROC	VSYS_VCORE	GND_VCORE	VCORE	VMODEM	GND_VMODEM					VS1_LDO1	C
D	AU_V18N	GND_VPROC_FB	VCORE_FB			D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	GND_VMODEM_FB		VRF18		D
E		FLYN	GND_VCORE_FB	VPA_FB		D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	VMODEM_FB	VS1_FB	VCN18	VRF12	VCAMD	E
F	FLYP	AVSS18_AUD	AU_LOLN	AU_LOLP	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND		VS2_LDO1		VS2_LDO2	F
G		AVDD18_AUD	AU_HPR		AU_HSN	AU_HSP	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND		VSYS_LDO1	VSRAM_PROC	VSRAM_OTHERS		G
H			AU_REFN		AVSS28_AUD	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND	D_GND			VEFUSE	VCAMA	VDRAM	H
J	HP_EINT	AU_HPL		AU_VIN2_P	AU_VIN2_N	D_GND	D_GND	D_GND	D_GND	DVSS18_IO	D_GND			VUSB			VSIM1	J
K	AVDD28_AUD		AU_VIN0_P	AU_VIN0_N	AU_VIN1_P		VSYS_LDO3			DVDD18_IO		D_GND	VCN28		VIO28	VSIM2		K
L			AU_MICBIAS0		AU_VIN1_N		VAUD28			DVDD18_DIG		ISINK1		VFE28	VMC	VLDO28	VEMC	L
M	XTAL1	AVSS22_XO	AU_MICBIAS1	ACCDET	EXT_PMIC_EN1	EXT_PMIC_PG	SPI_MOSI	SPI_CLK	SPI_MISO	CHG_DM	CHG_DP		BATSNS	AUD_SYNC_MOSI		VIBR		M
N	XTAL2	AVSS22_XO_ISO	UVLO_VTH	FCHR_ENB	EXT_PMIC_EN2		SRCLKEN_IN0	SRCLKEN_IN1	VSYSSNS			PCHR_LED	ISENSE	AUD_DAT_MOSI1		VMCH	VSYS_LDO2	N
P	AVSS22_XOBUF	AVSS22_XO_ISO	XO_WCN		PMU_TESTMODE		AVSS18_AUXADC		FSOURCE		RTC32K_2V8		VDRV	RTC32K_1V8_0	AUD_DAT_MOSI0	AUD_CLK_MOSI	VCN33	P
R	AVSS22_XOBUF	XO_NFC	XO_SOC	PWRKEY	RESETB		AVDD18_AUXADC	SPI_CSN	TREF	CS_N	CHRLDO	VRTC28	BATON		RTC32K_1V8_1	AUD_CLK_MISO	AUD_DAT_MISO1	R
T	XO_CEL	XO_EXT		VXO22	VAUX18		AUXADC_VIN	WDTRSTB_IN		CS_P	VCDT		GND_VREF	VREF		AUD_SYNC_MISO	AUD_DAT_MISO0	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

Legend
Power Input
Buck Output
Buck_GND
LDO Input
LDO Output
GND
Audio
AuxADC
RTC
Charge
DCXO

MT6357 Power Input (1/2)

VSYS Input

- VSYS 22uF capacitor is placed near MT6357 **VSYS** input balls (Fig. 2).
- Routing from 22uF VSYS capacitor uses start topology to connect to each device.
  1. **VSYS** input for BUCK. (Fig. 3)
  2. **VSYS** input for LDO. (Fig. 3)
- Follow the trace width rule in Fig. 4.
- All the decoupling capacitors should be placed near MT6357. The priority is buck capacitor then decoupling capacitor of LDO. (Fig.1)

Fig. 4

IC Ball Name	IMAX(mA)
VSYS_VPROC	~~3031~~ 3384
VSYS_VCORE	~~2520~~ 3600
VSYS_VMODEM	~~2000~~ 1670
VSYS_VS1	2500
VSYS_VPA	1750
VSYS_LDO1	2000
VSYS_LDO2	2000
VSYS_LDO3	2000

Fig. 1

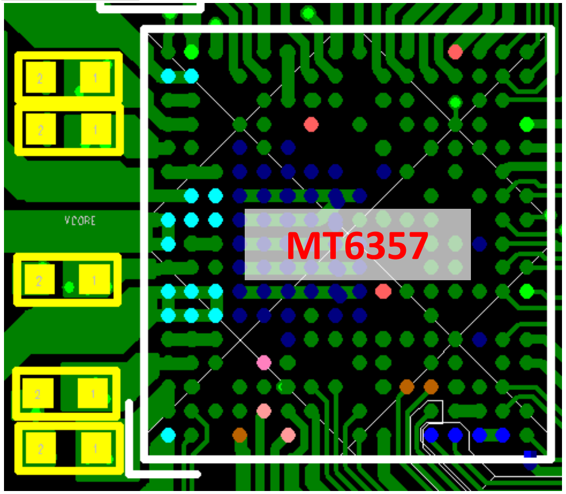


Fig. 2

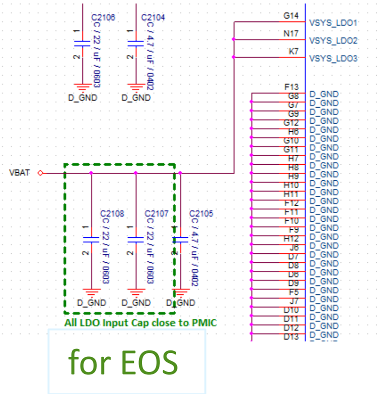
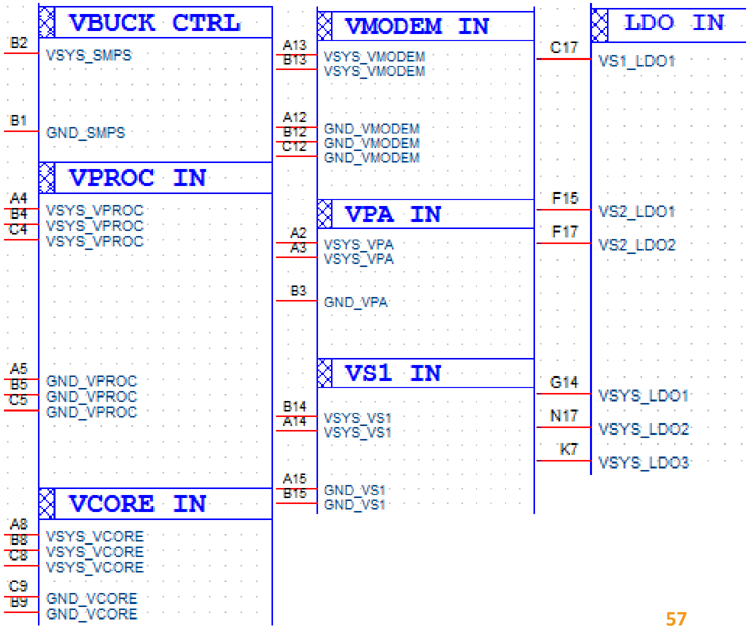


Fig. 3



MT6357 Power Input (2/2)

- **Layout method of MT6357 power Input for Buck GND**
  - Buck GND balls are connected to buck capacitors close to pin with plane or trace (Trace Width > **8mil * N (ball number) + M (ball pitch)**). (Fig.1~2)
  - Buck GND balls should be connected to buck capacitors first and isolated from the nearby GND trace and plane then connected to main GND at L3 (Fig.1~2).

Fig.1

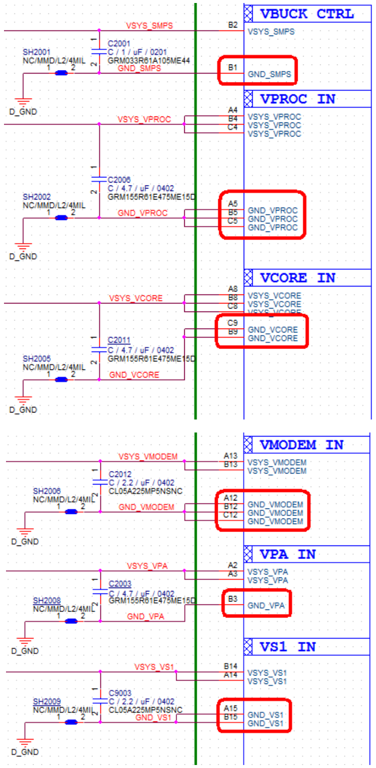
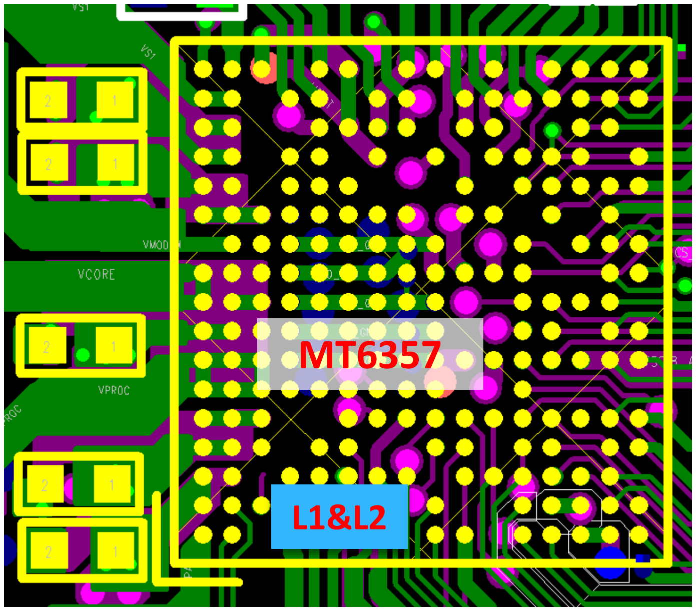
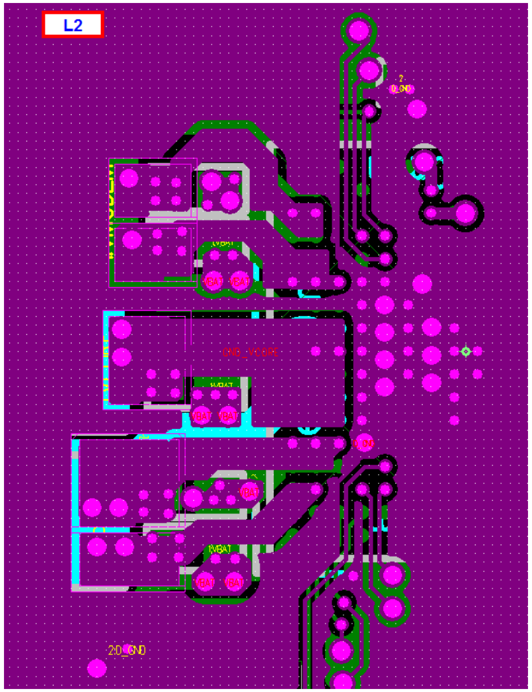


Fig.2





Layer 2: BUCK GND is isolated from nearby GND trace and plane.

MT6357 Buck Output (1/2)

- The buck inductors should be placed near MT6357. (Fig.1)
- The output current is shown in Fig.2.

Fig.1

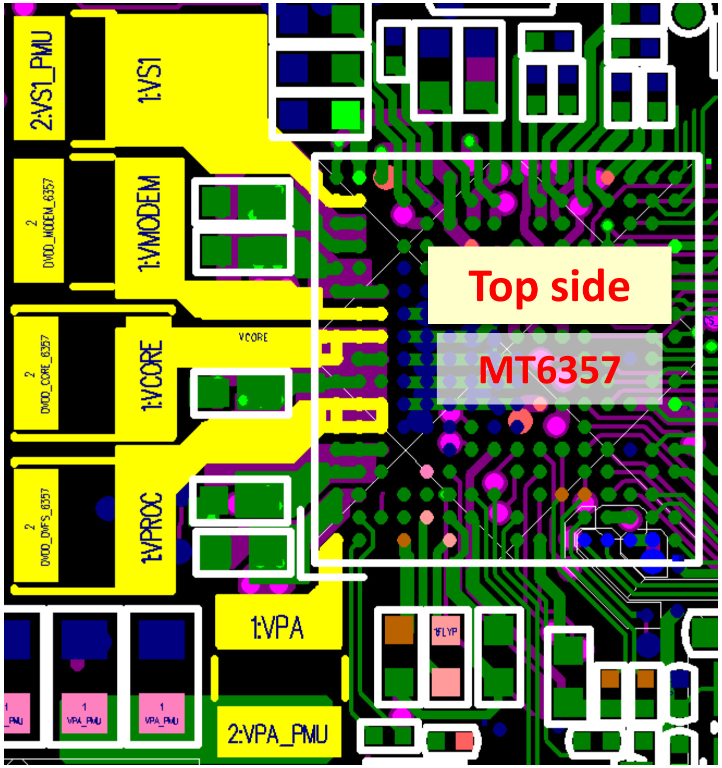
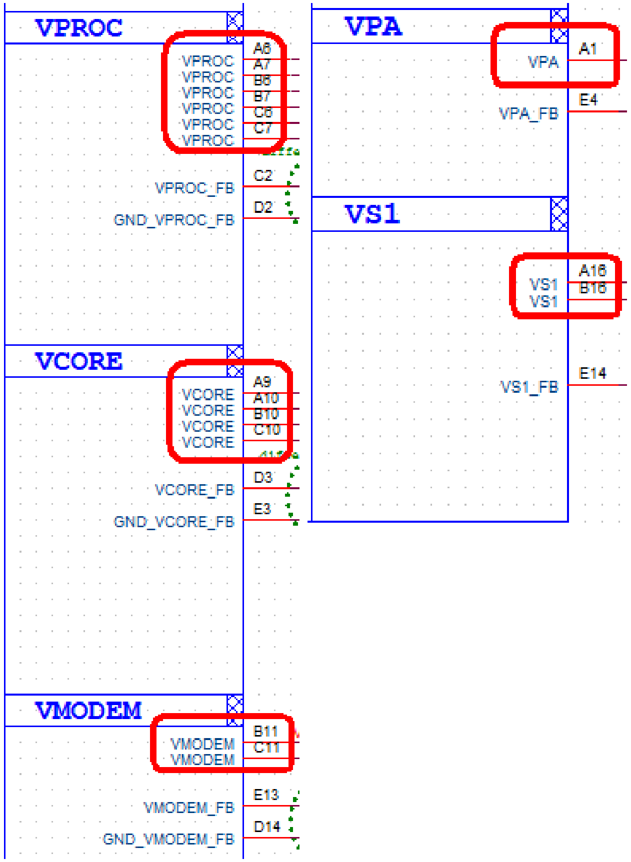


Fig.2

Output ball name	Output current (mA)
VMODEM	2500
VPROC	4210
VCORE	3500
VS1	1900
VPA	1750



MT6357 Buck Output (2/2)

- Those signals are differential pairs and should be shielded by GND and far away from noise signals (Fig.1 ~ Fig.2).
  1) VMODEM_FB/GND_VMODEM_FB
  2) VPROC_FB/GND_VPROC_FB
  3) VCORE_FB/GND_VCORE_FB
  4) VPA_FB , VS1_FB

Fig. 2

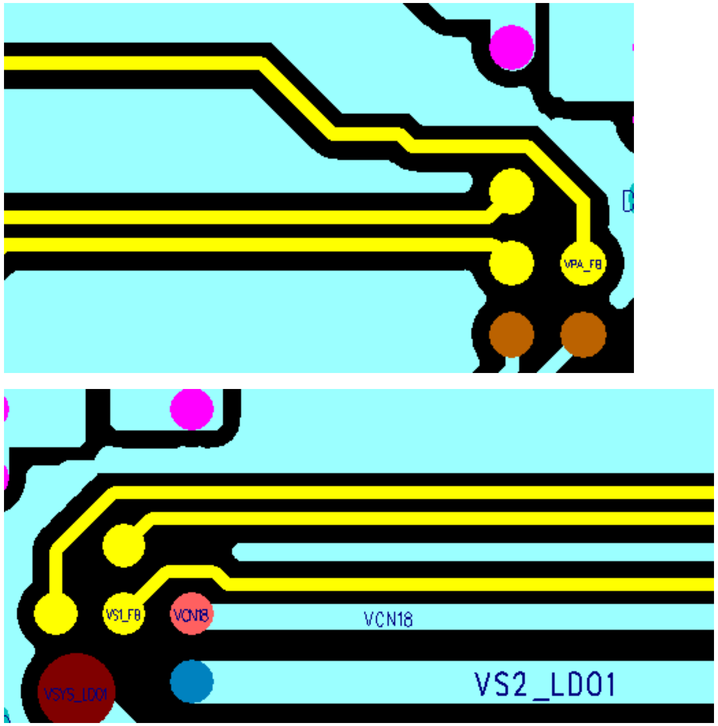
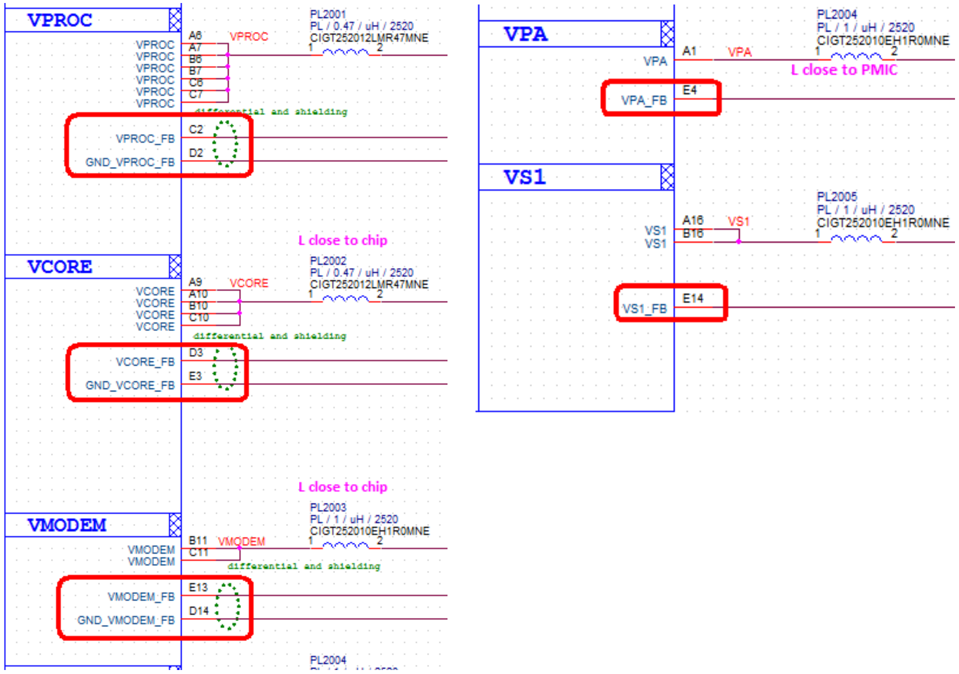
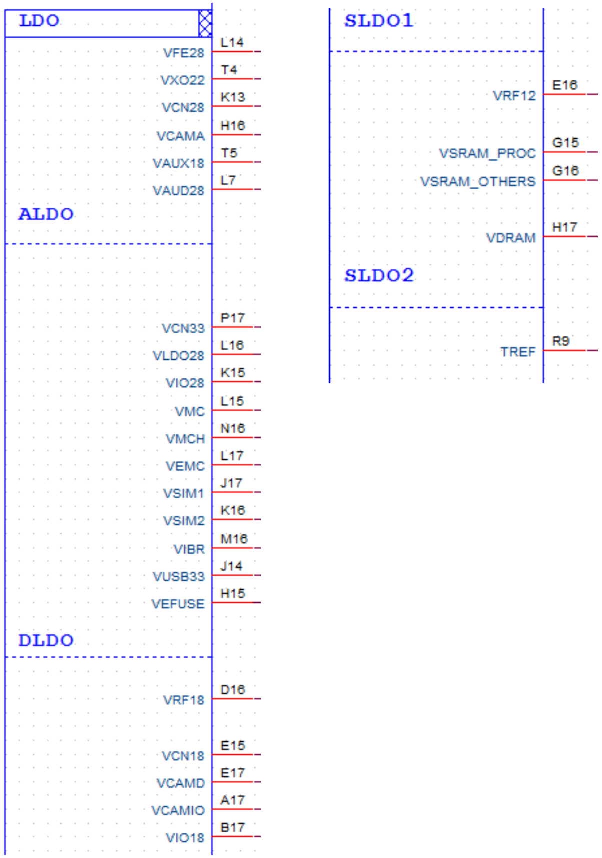


Fig. 1



MT6357 LDO Output (1/2)

- See Fig. 1 for the suggested LDO output layout.



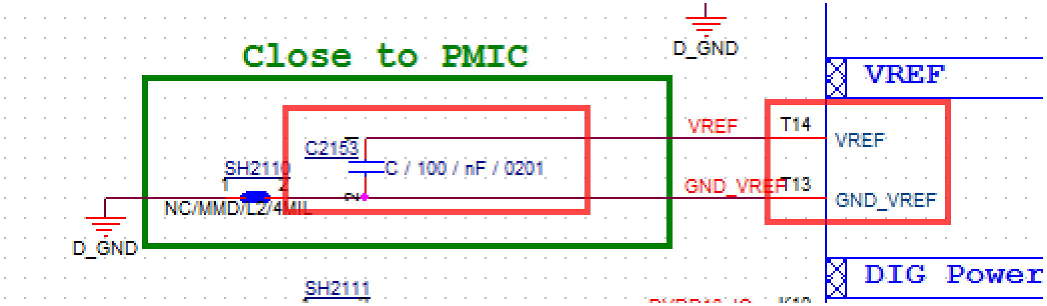
LDO output layout suggestion

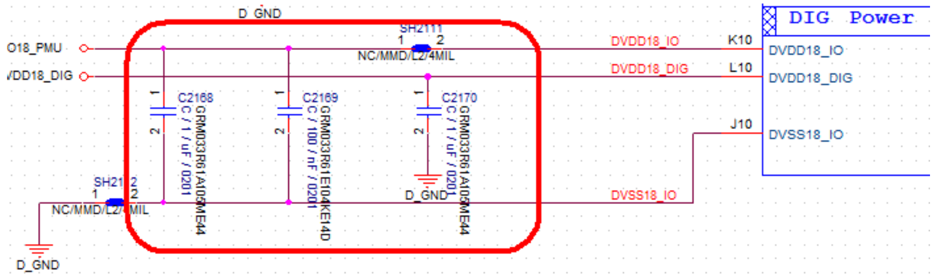
Ball name	Width/Trace length	I_{MAX} (mA)
VFE28	6mil/2500mil	40
VXO22	6mil/2500mil	25
VCN28	6mil/2500mil	40
VCAMA	8mil/3000mil	146
VAUX18	6mil/2500mil	20
VAUD28	6mil/2500mil	50
VCN33	12mil/1000mil	400
VLDO28	12mil/3000mil	360
VIO28	8mil/3000mil	200
VMC	8mil/3000mil	200
VMCH	20mil/1000mil Under Chip: Layout Length < 30mil	800
VEMC	12mil/1000mil	400
VSIM1	6mil/2500mil	50
VSIM2	6mil/2500mil	50
VIBR	6mil/2500mil	100
VUSB	6mil/2500mil	50
VEFUSE	8mil/3000mil	200
VRF18	All traces should be in inner layer or under shielding case. 14mil/1000mil near-end cap: 4.7µF@L<7nH 14mil/3000mil middle-end cap: 4.7µF@L<20nH	450
VCN18	8mil/3000mil	200
VCAMD	14mil/3000mil	350
VCAMIO	8mil/3000mil	143
VIO18	16mil/1000mil	600
VRF12	All traces should be in inner layer or under shielding case. 8mil/1000mil near-end cap: 4.7µF@L<7nH 8mil/3000mil middle-end cap: 4.7µF@L<20nH	200
VSRAM_PROC	8mil/1000mil near-end cap: 2.2µF@L<7nH	150
VSRAM_OTHERS	8mil/1000mil near-end cap: 2.2µF@L<7nH	190
VDRAM	30mil/1000mil	1200
TREF	6mil/2030mil	1

MT6357 LDO Output (2/2)

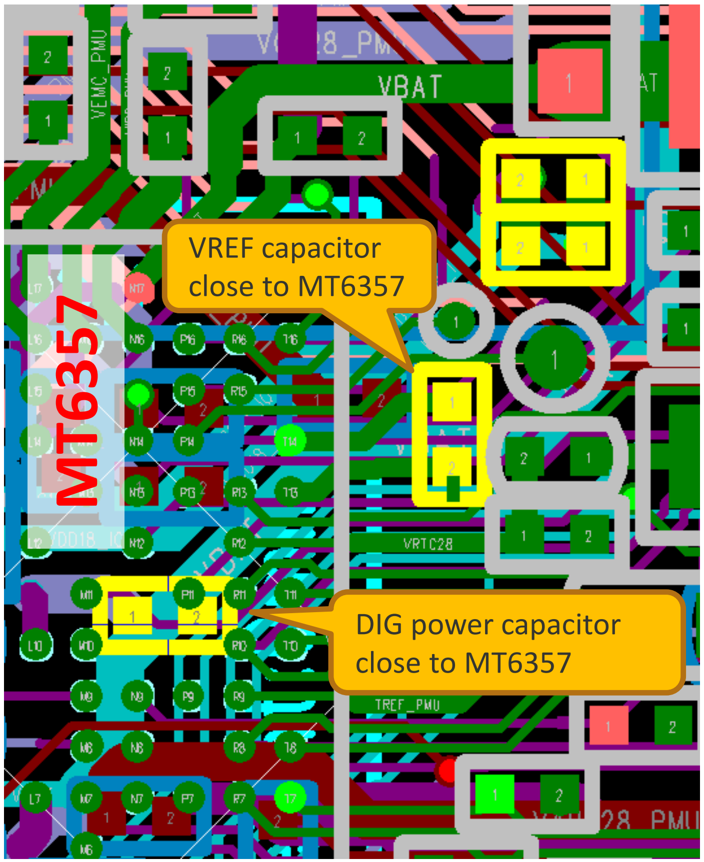
- VREF capacitor should be placed near T13/T14 pin.
- DVDD18_DIG capacitor should be placed near L10 pin.

Update C2153 to 100nF from 1uF





Close to MT6357



MT6357 Audio (1/3)

- The signals in Table 1 should be routed as differential pairs and shielded by GND (adjacent and up/down layers) and trace width ≧ 4mil.
- AU_HPR/AU_HPL signals should be shielded by GND respectively and trace width ≧ 6mil.
- Other signals should be routed orthogonally to other signals between adjacent layers.
- Related capacitors should be placed near MT6357. (Fig. 1 ~ Fig. 4)

Table 1

Ball number	PCB net name	IC ball name
K3	AU_VIN0_P	AU_VIN0_P
K4	AU_VIN0_N	AU_VIN0_N
K5	AU_VIN1_P	AU_VIN1_P
L5	AU_VIN1_N	AU_VIN1_N
J4	AU_VIN2_P	AU_VIN2_P
J5	AU_VIN2_N	AU_VIN2_N
G5	AU_HSN	AU_HSN
G6	AU_HSP	AU_HSP
G3	**AU_HPR**	**AU_HPR**
J2	**AU_HPL**	**AU_HPL**
F4	**AU_LOLP**	**AU_LOLP**
F3	**AU_LOLN**	**AU_LOLN**

Fig.1

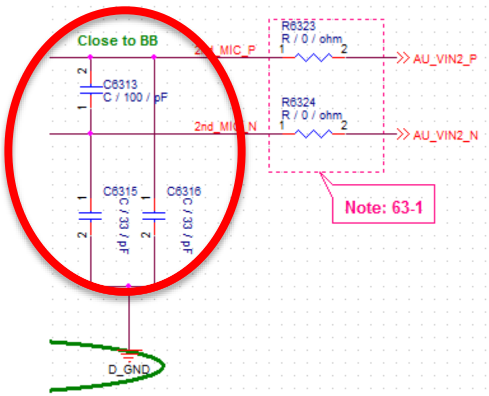


Fig.2

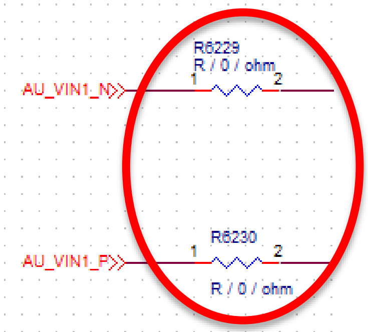


Fig.3

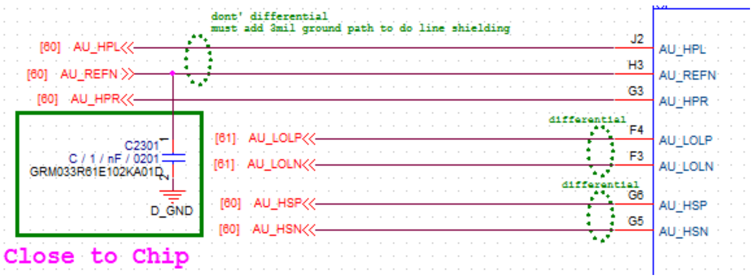
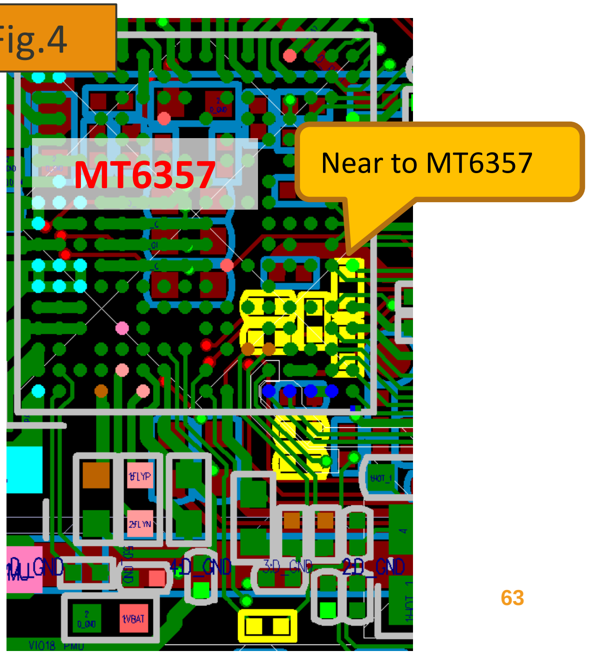


Fig.4



MT6357 Audio (2/3)   Power

- Audio Negative Charge Pump (AUDNCP) related pins: AVDD18_AUD/AVSS18_AUD/AN_V18N/ FLYP/FLYN
  - All traces are wide and short. To minimize ESR and ESL, all traces are on TOP layer without any PCB via. Avoid using PCB VIA between the 5 traces (from ball to cap). (Fig.1 ~ Fig.2)
  - AVSS18_AUD should be connected to main GND with very short trace. (Fig.1 ~ Fig.2)
- AVDD28_AUD and AVSS28_AUD domain, the decoupling cap should also be as close to chip as possible. AVSS28_AUD is connected to main GND with a single VIA. (Fig.3)

Fig.1

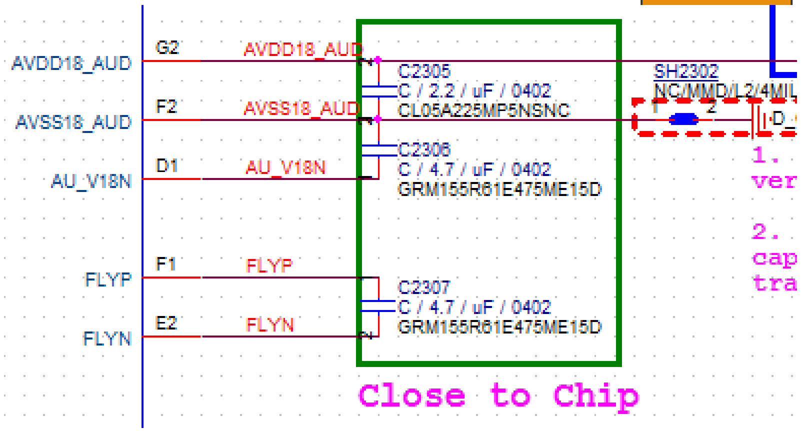
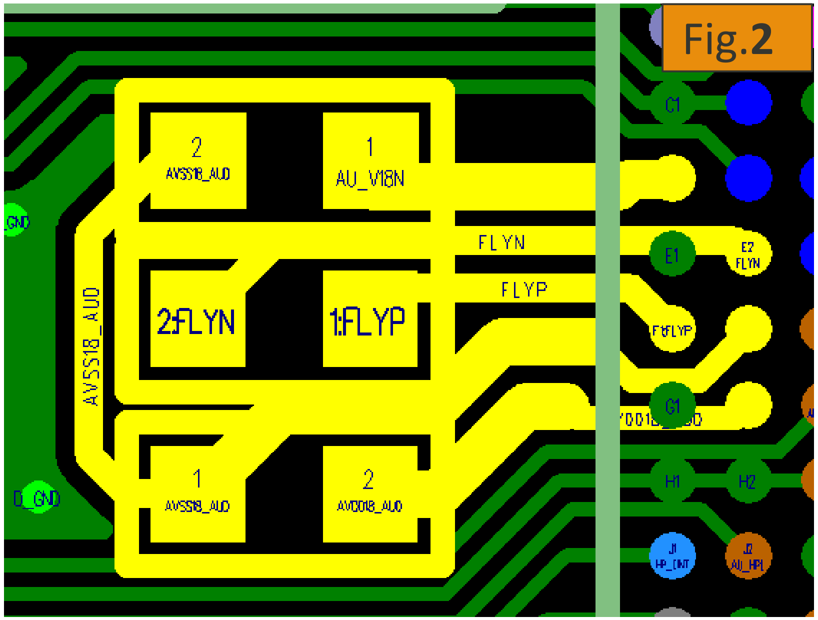


Fig.2



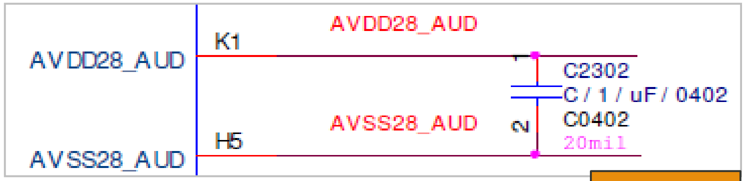
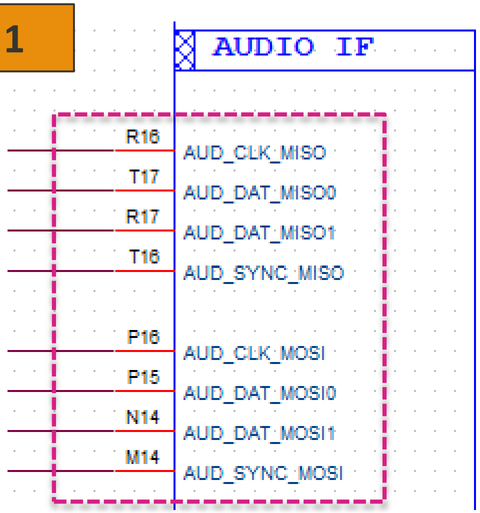


Fig.3

MT6357 Audio (3/3)
Audio/CLK IF Schematic and Layout Notice

- The trace length of AUD_CLK_MOSI/AUD_DAT_MOSI0/AUD_DAT_MOSI1/AUD_SYNC_MOSI should be the same as much as possible.
- The trace length of AUD_CLK_MISO/AUD_DAT_MISO0/AUD_DAT_MISO1/AUD_SYNC_MISO should be the same as much as possible.
- AUD_CLK_MOSI/AUD_CLK_MISO should have GND shielded and the spacing should be >= 3mil.
- Audio IF should be kept away from LX signal (e.g. VCORE) and CLK. (Fig. 1)

Fig.1

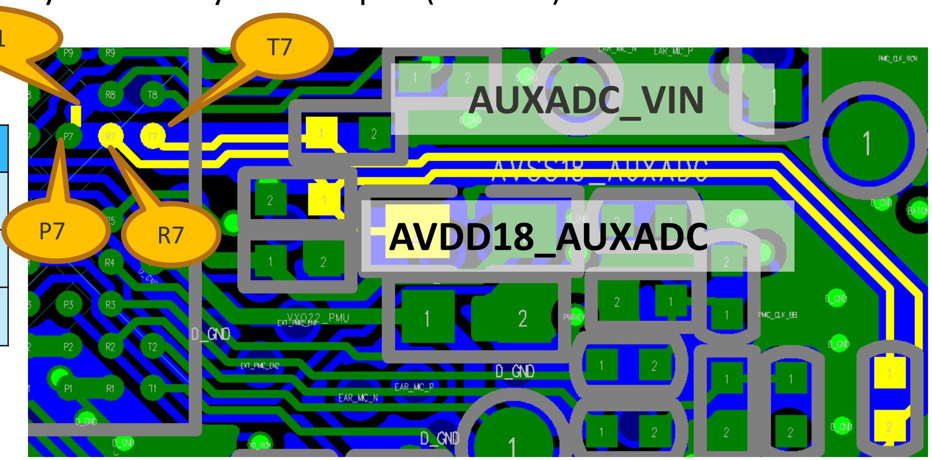


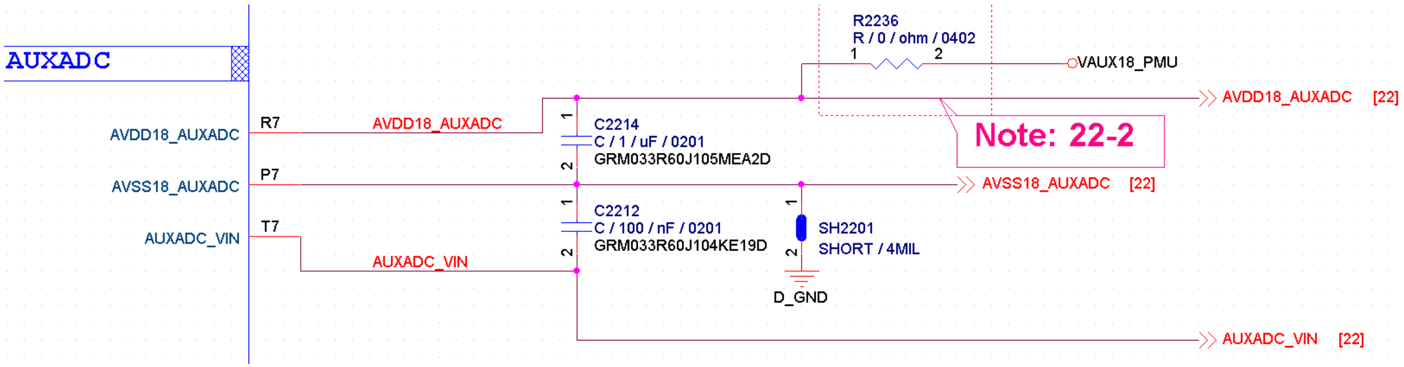
MT6357 AUXADC

Recommended AUXADC layout

- Route AVDD18_AUXADC, AUXADC_VIN, and AVSS18_AUXADC with 3mils width traces and well GND shielding
- Use AVSS18_AUXADC or GND for AVDD18_AUXADC and AUXADC_VIN shielding.
- AUXADC capacitor should be placed near AVDD18_AUXADC/AUXADC_VIN pin.
- Please connect the AVSS18_AUXADC to GND by a inner-layer short-pad (SH2201).

Ball number	IC ball name	PCB net name
R7	AVDD18_AUXADC	AVDD18_AUXADC
P7	AVSS18_AUXADC	AVSS18_AUXADC
T7	AUXADC_VIN	AUXADC_VIN

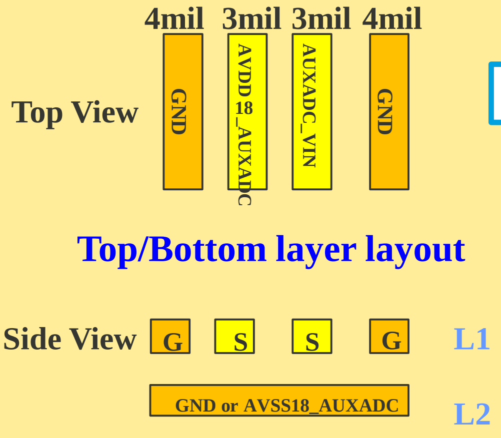


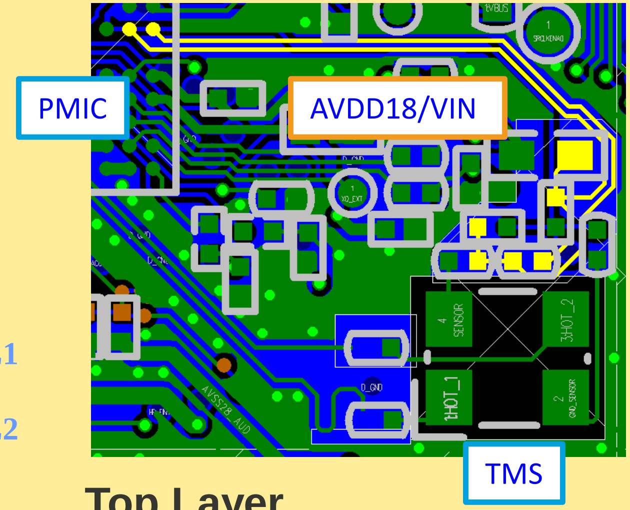


Example: AUXADC Trace Routing

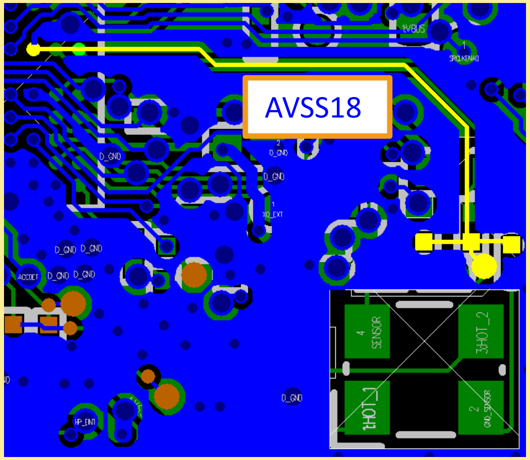
1. **(Recommended)** Routed **AVDD18/VIN** on the **top layer** and **AVSS** on the **2nd layer**.

AVDD18_AUXADC/AUXADC_VIN on the top and AUXADC_GND on 2nd layer



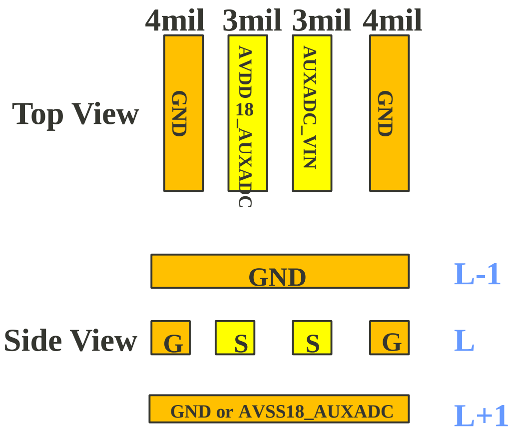


Top Layer



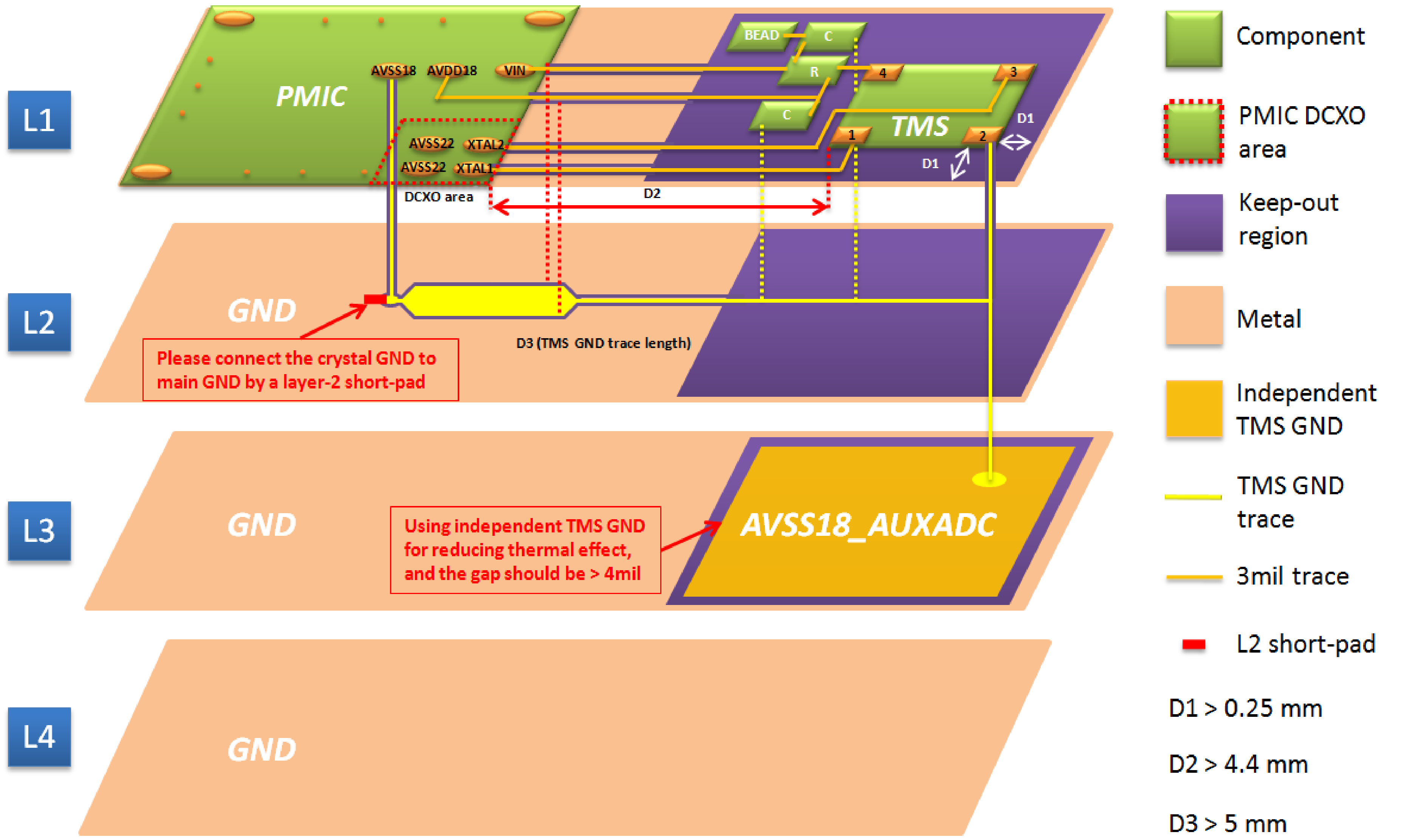
2nd layer

2. Routed in inner Layer is doable, and let AUXADC two traces with well-ground shielding by GND or AVSS18_AUXADC.



PMIC with Co-TMS Layout Recommendation

Keep the TMS and PMIC DCXO area > 10 mm away from PAs



MT6357 DCXO (1/2)

- XTAL1 and XTAL2 connection to TMS pin 1 and pin 3 can be swapped. Keep out Buck, NCP, Class-D or other toggling signals 9mm away. (Fig.1)
- Short DCXO gnds to main GND directly by the GND vias. (Fig.2)

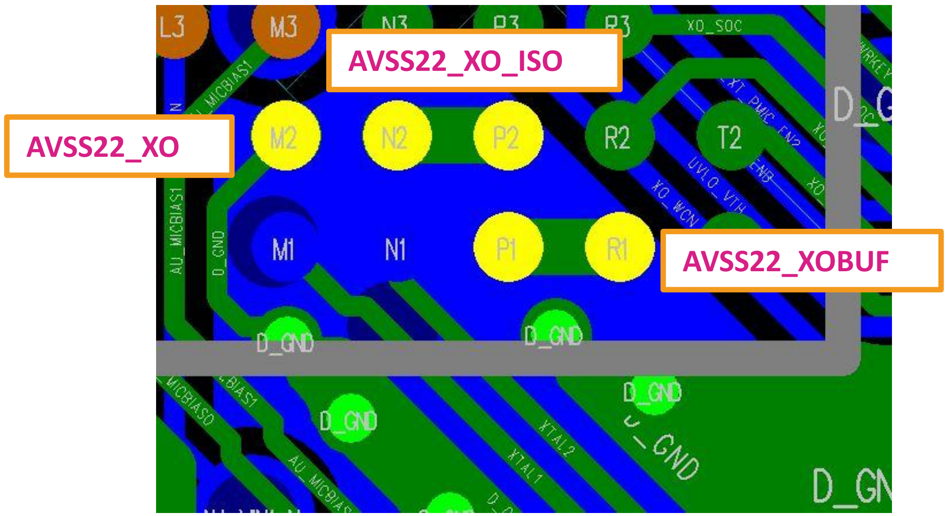
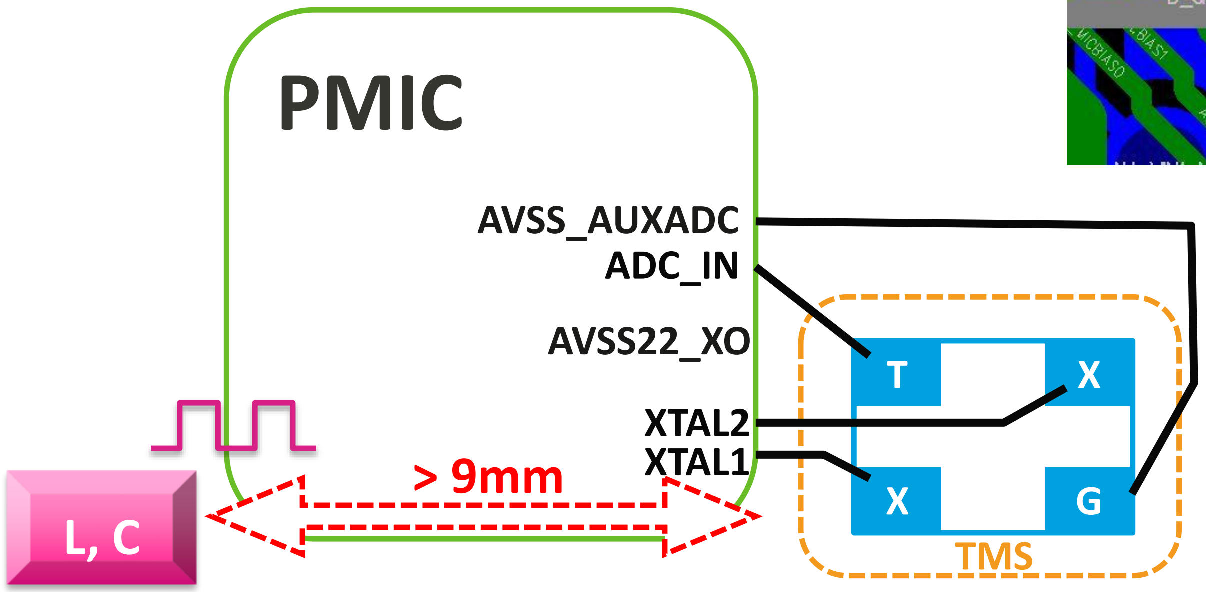


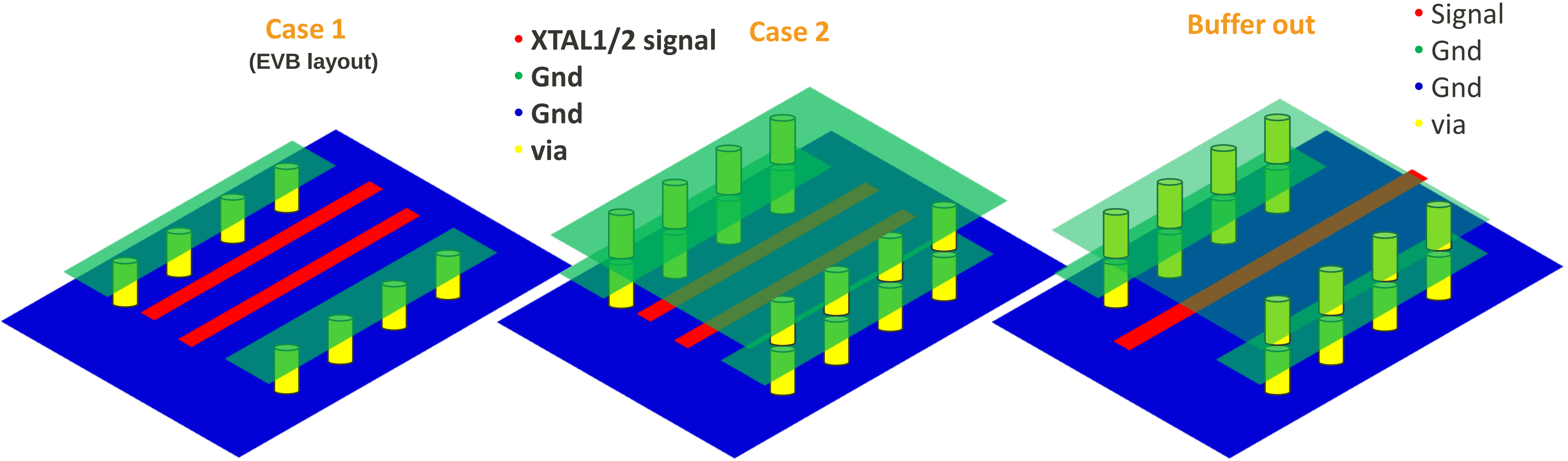
Fig. 2

Fig. 1



MT6357 DCXO (2/2)

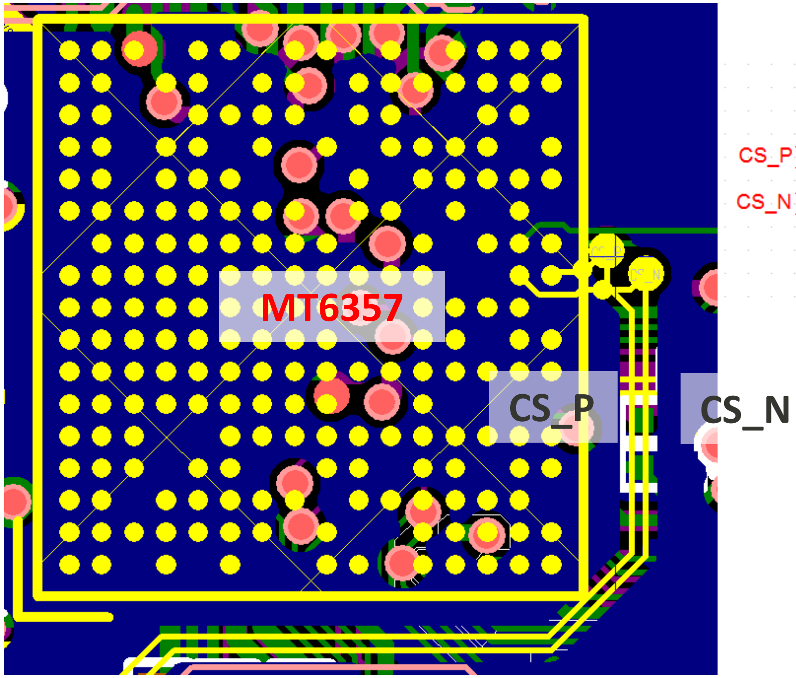
- **XTAL1/2 shielding case 1**
  - Route XTAL1/2 on the 1st layer, with well-grounding in the 1st and 2nd layers.
  - Any other signals crossing or parallel XTAL1/2 are not allowed.
- **XTAL1/2 shielding case 2**
  - Well shielding XTAL1/2 (2nd layer) with GND
  - Any other signals crossing or parallel XTAL1/2 are not allowed.
- Separate ground shielding for each buffer output, XO_SOC, XO_WCN, XO_NFC, XO_CEL, XO_EXT.

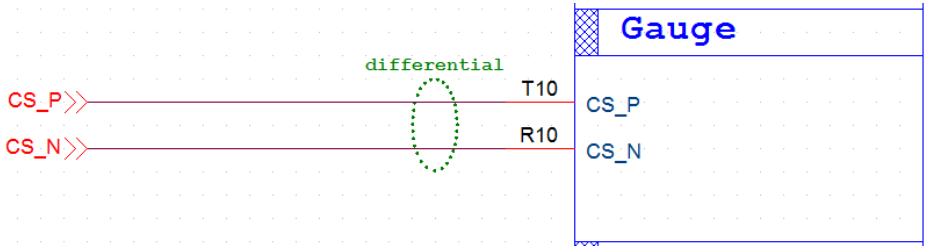


Others for MT6357

Gauge

- CS_N/CS_P (ball: R10/T107) should be routed as differential pairs and far away from noise signals.



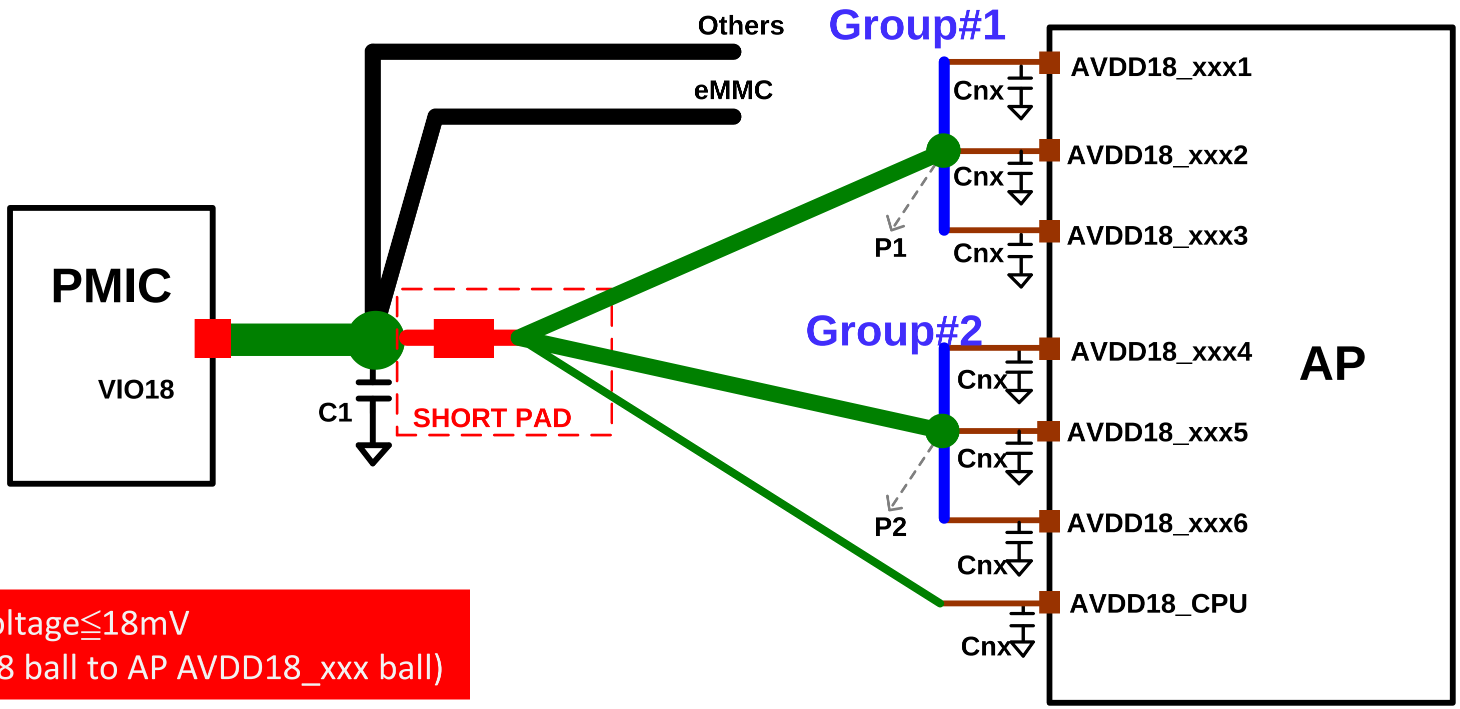


AP Analog and Power List

Voltage	PMIC Pin Name	Group#1 (AP analog pin name)	Group#2 (AP analog pin name)
1.8V	VIO18	AVDD18_MD, AVDD18_AP, AVDD18_WBG	AVDD18_USB, AVDD18_PLLGP, AVDD18_CPU
1.2V	VA12	AVDD12_MD, AVDD12_DSI, AVDD12_USB,	AVDD12_CSI, AVDD12_PLLGP, AVDD12_WBG
3.075V	VUSB	AVDD33_USB	N/A

AP AVDD18_xxx Layout Constraint

Group#1: AVDD18_MD, AVDD18_AP, AVDD18_WBG
Group#2: AVDD18_USB, AVDD18_SSUSB, AVDD18_PLLGP, AVDD18_UFS



PCB drop voltage≦18mV
(PMIC VIO18 ball to AP AVDD18_xxx ball)

Example		Average current	PCB Width	PCB Length	PCB Thickne	PCB Resister	PCB drop voltage
Trace Start	Trace End						
PMIC VIO18 ball	C1	0.600A	20mil	200mil	0.3oz	17.7m	10.6mV
C1	P2	0.085A	20mil	800mil	0.3oz	71.0m	6.0mV
P2	AP AVDD18_USB ball	0.030A	12mil	300mil	0.3oz	44.3m	1.3mV

Pass ≦18mV

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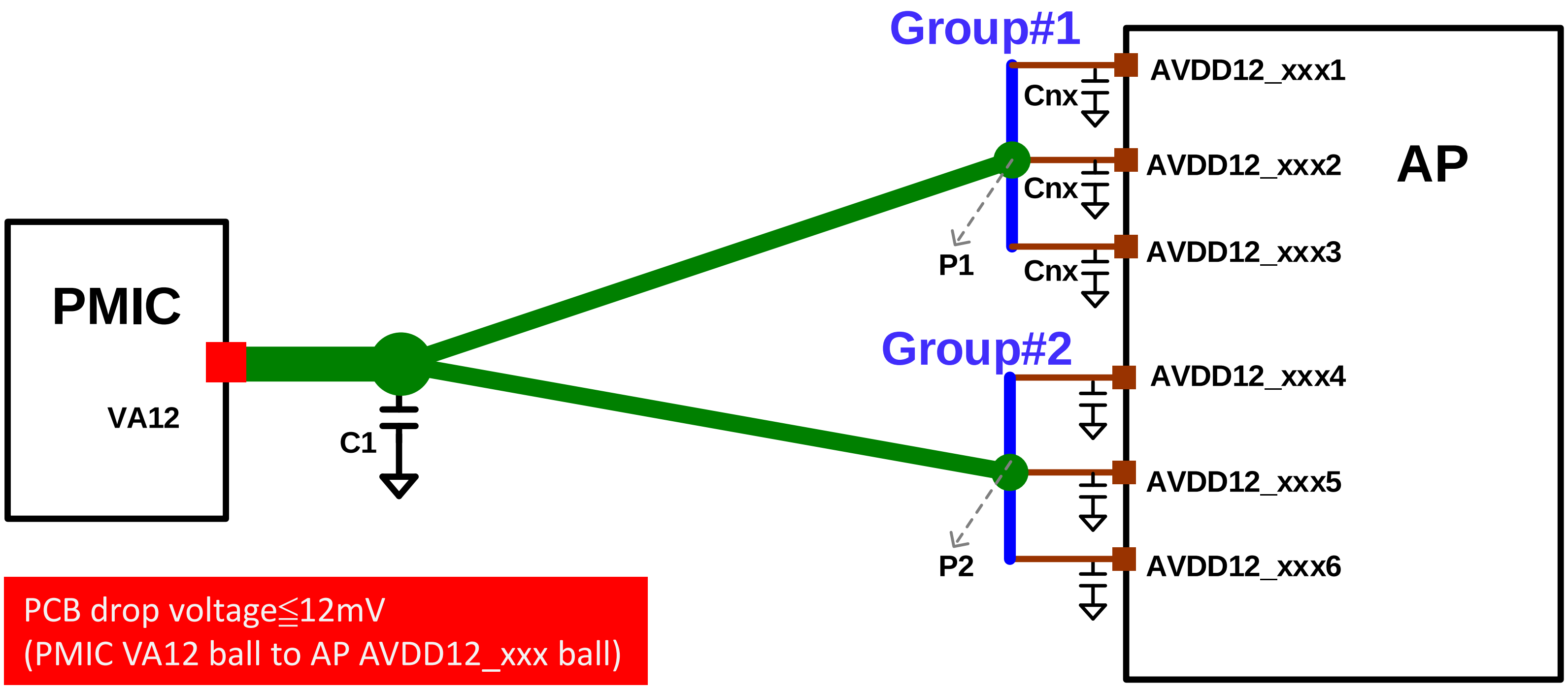
AP AVDD12_xxx Layout Constraint

Group#1: AVDD12_MD,AVDD12_DSI,AVDD12_USB,AVDD12_UFS
Group#2: AVDD12_CSI,AVDD12_PLLGP,AVDD12_WBG



PCB drop voltage≦12mV
(PMIC VA12 ball to AP AVDD12_xxx ball)

for layout example		Average current	PCB Width	PCB Length	PCB Thicknes	PCB Resister	PCB drop voltage
Trace Start	Trace End						
PMIC VA12 ball	C1	0.120A	14mil	250mil	0.3oz	31.7m	3.8mV
C1	P1	0.060A	14mil	800mil	0.3oz	101.4m	6.1mV
P1	AP AVDD12_MD ball	0.040A	6mil	200mil	0.3oz	59.1m	2.4mV

Pass ≦12mV

AP AVDD33_USB Layout Constraint

PCB drop voltage≦30mV
(PMIC VUSB ball to AP AVDD33_USB ball)

for layout example		Average current	PCB Widt	PCB Length	PCB Thickne	PCB Resister	PCB drop voltage
Trace Start	Trace End						
PMIC VUSB ball	C1	0.05A	8mil	500mil	0.3oz	110.9m	5.5mV
C1	AP AVDD33_USB ball	0.05A	8mil	2000mil	0.3oz	443.4m	22.2mV

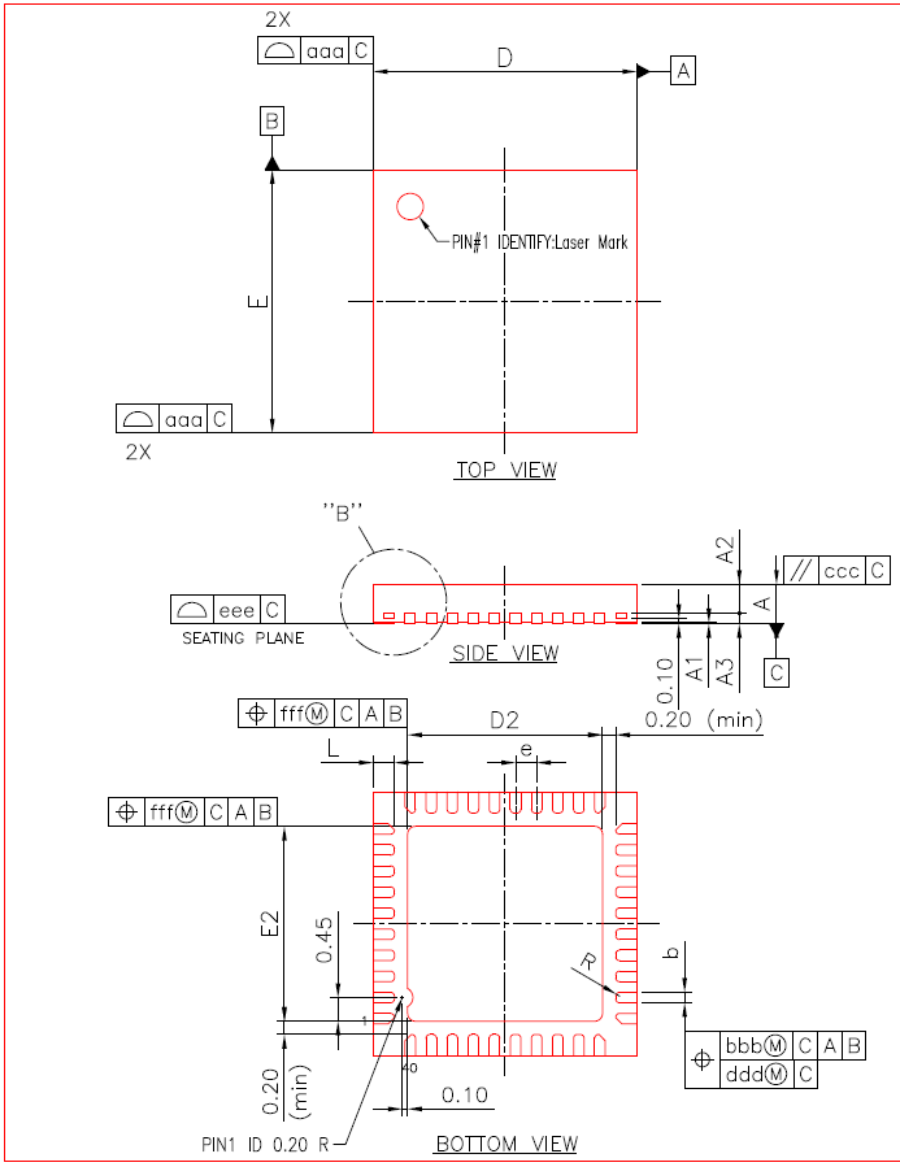
Pass ≦30mV

Outlines

- **Packaging**
  - Package outline of MT6765
  - MT6765 footprint recommendation
  - MT6765 ball out design
- **General Guidelines**
  - PCB stack-up recommendation
  - Placement notes
- **Design Guidelines for High-speed Digital Signals**
  - LPDDR4X/LPDDR3
  - PDN design
- **Others**
  - MT6765 RF interface - MT6177 (RF transceiver)
  - MT6765 RF interface - MT6177M (RF transceiver)
  - MT6357 (PMU)
  - MT6631 (BT/FM/Wi-Fi/GPS)
  - MT6371 (battery charger/USB_PD)
  - eMMC/USB/MIPI/SIM card/T-card

MT6631
PCB Layout Guideline

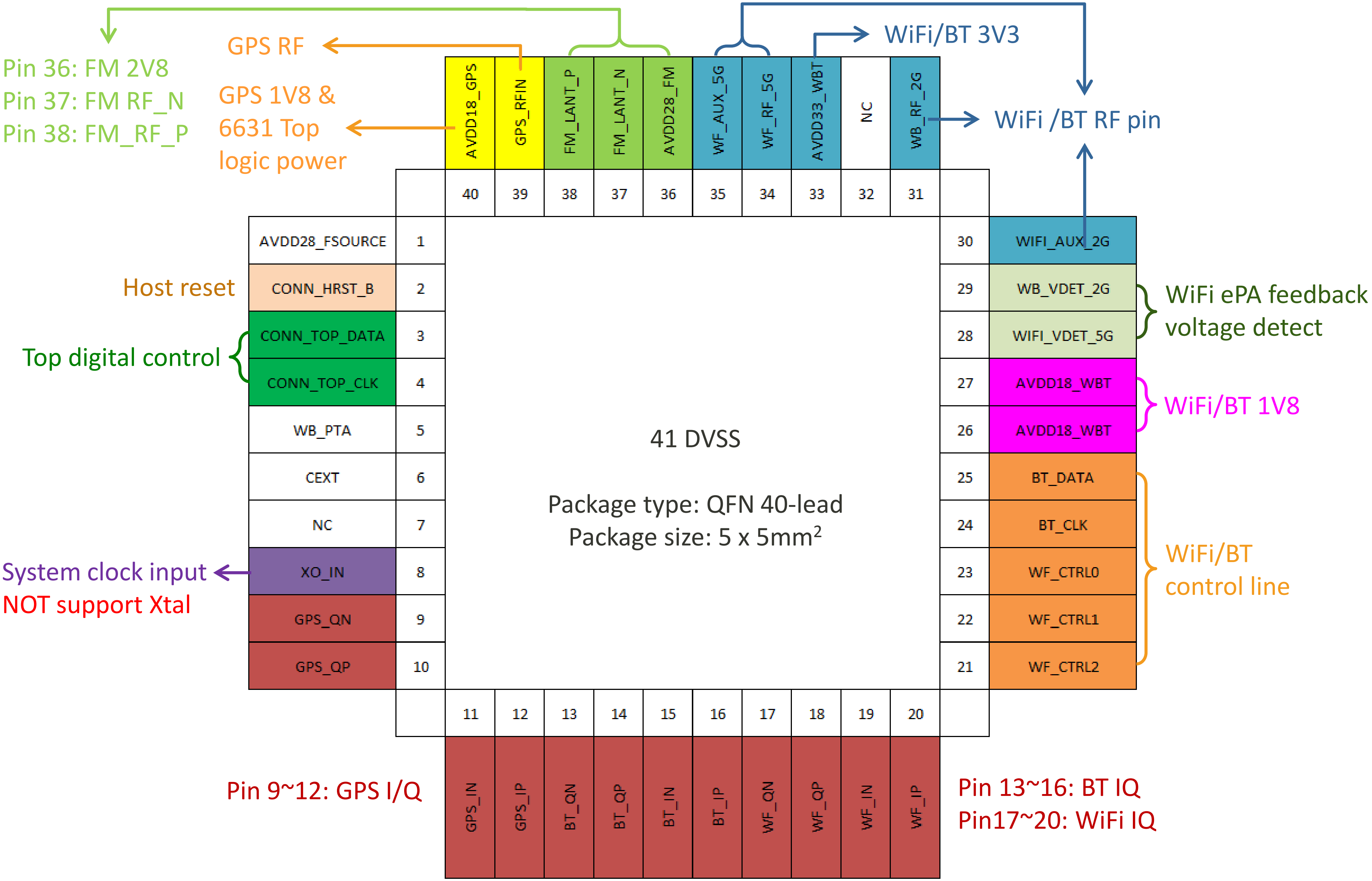
Package Outline of MT6631



Item		Symbol	MIN.	NOM.	MAX.
total height		A	0.70	0.75	0.80
stand off		A1	0.00	0.02	0.05
mold thickness		A2	0.50	0.55	0.60
leadframe thickness		A3	0.20 REF.		
lead width		b	0.15	0.20	0.25
package size	X	D	4.90	5.00	5.10
	Y	E	4.90	5.00	5.10
E-PAD size	X	D2	3.60	3.70	3.80
	Y	E2	3.60	3.70	3.80
lead length		L	0.30	0.40	0.50
lead pitch		e	0.40 bsc		
lead arc		R	0.075	---	---
Package profile of a surface		aaa	0.10		
Lead position		bbb	0.07		
Paralleliam		ccc	0.10		
Lead position		ddd	0.05		
Lead profile of a surface		eee	0.08		
Epad position		fff	0.10		

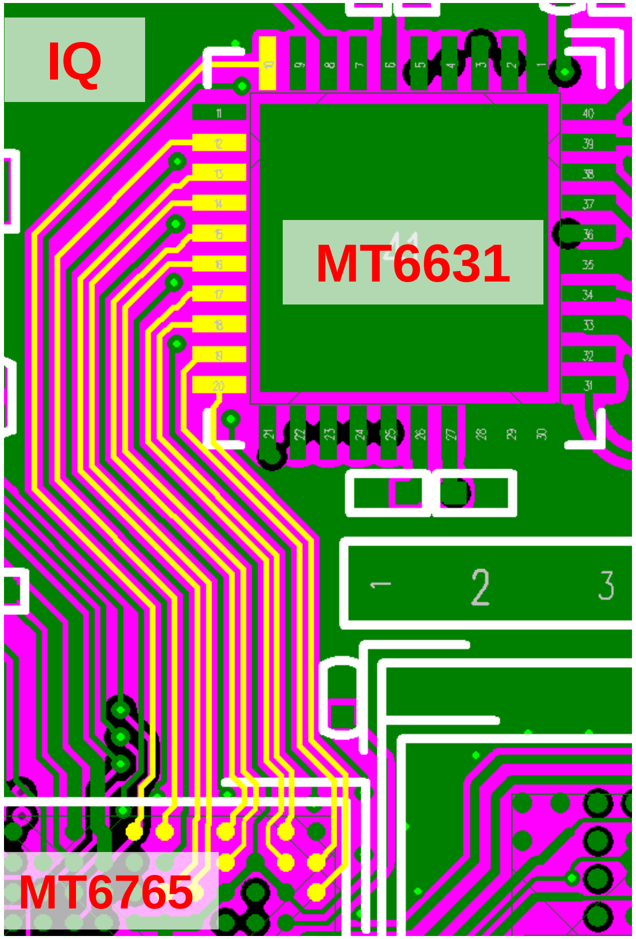
TITLE	PACKAGE OUTLINE 40 L WSQFN 5 X5 X 0.8 mm		MEDIATEK	
	DWG. NO.	REV.	SHEET	UNIT
	MT-SP00329	A	1 OF 2	MM

MT6631 Pin Definition



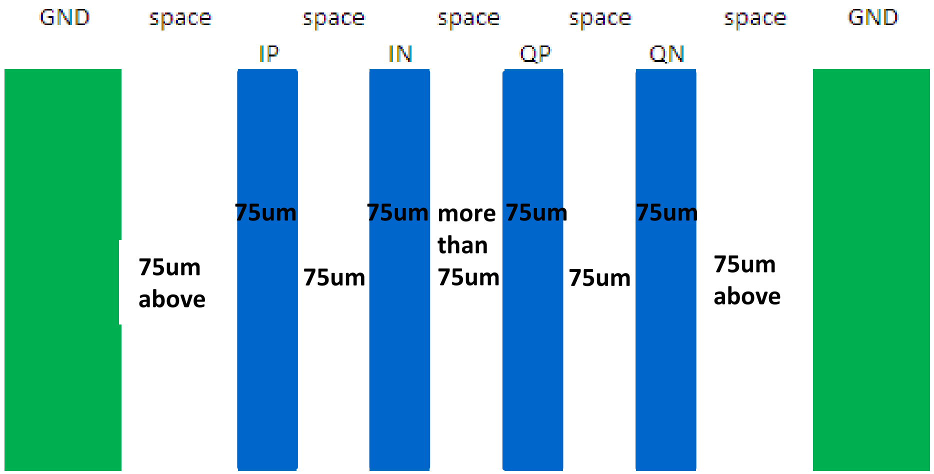
MT6631 vs. MT6765 Placement

- Keep the distance between MT6631 and MT6765 between 0.7cm~5cm.
  - If < 0.7cm: It may cause connectivity RF de-sense.
  - If > 5cm: IQ signals will be distorted (like EVM fail, Critical).



MT6631 IQ Trace

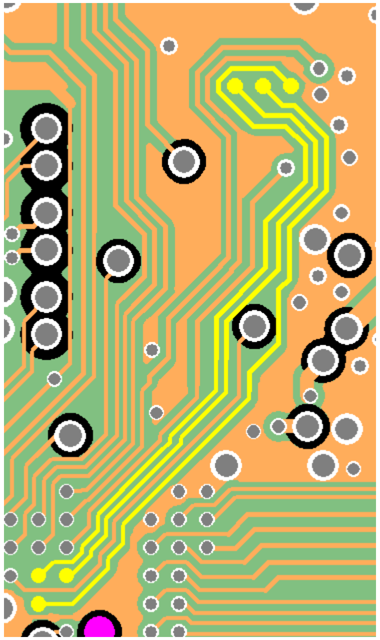
- IQ signals are differential pairs. Every pair should be shielded by GND (adjacent and up/down layers). If the layout area is not enough, shield by groups, for example:
  - WiFi group: WF_IP/IN/QP/QN Pin 17 ~ Pin 20
  - BT group: BT_IP/IN/QP/QN Pin 13 ~ Pin 16
  - GPS group : Use single-end GPS_IP/QP signal for GPS, GPS: IN/QN:NC (Pin 9 &Pin 11)
- IQ trace width/spacing: 75/75um differential pair. PCB trace should be as balanced as possible, and keep differential signals balanced. Smallest differential loop area.
- Spacing 75um above with GND



MT6631 Control Trace

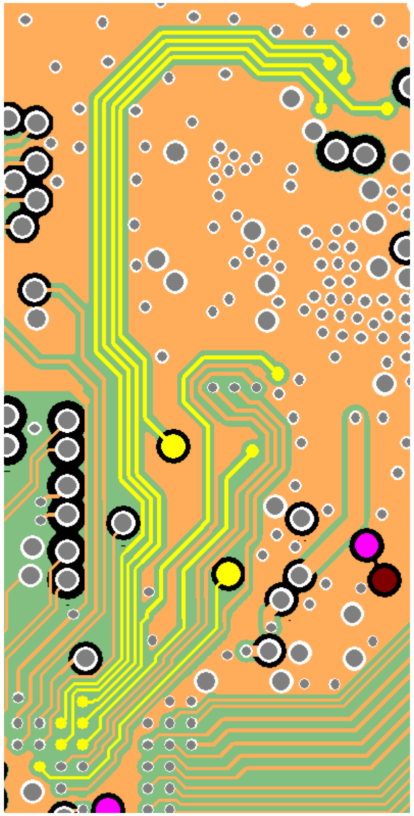
- **High-speed connectivity WF 3-wire control line**
  - Routed together and shielded by GND for left and right.
  - Do not couple with Power Line and IQ trace, and route in inner layer away from WiFi/GPS RF trace.

Group	Pin no.	PCB net-name
WF_CTRL	23	WF_CTRL0
	22	WF_CTRL1
	21	WF_CTRL2



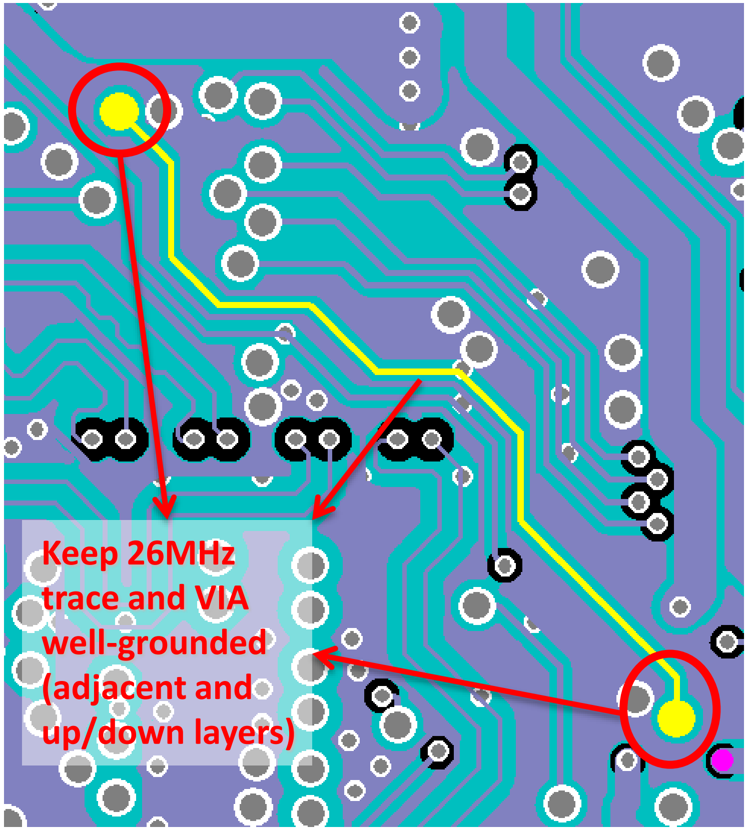
- **Other control signals**
  - Routed in inner layer; do not couple with Power Line and IQ trace.

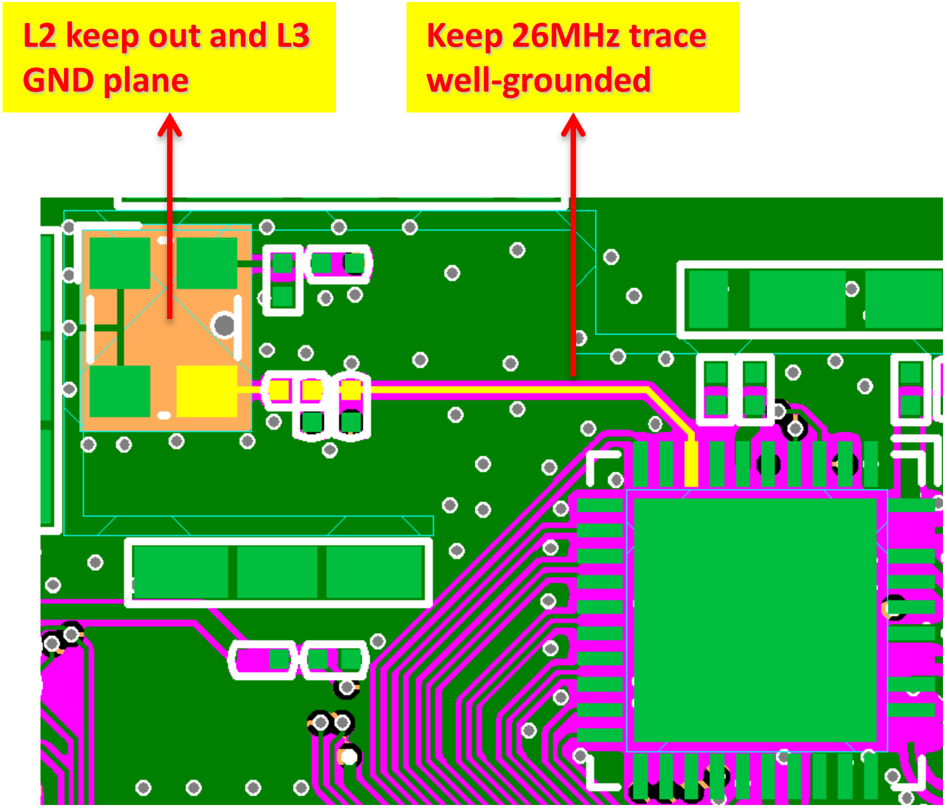
Group	Pin no.	PCB net-name
Other control signals	2	CONN_HRST_B
	3	CONN_TOP_DATA
	4	CONN_TOP_CLK
	5	WB_PTA
	24	BT_CLK
	25	BT_DATA



MT6631 26MHz CLK

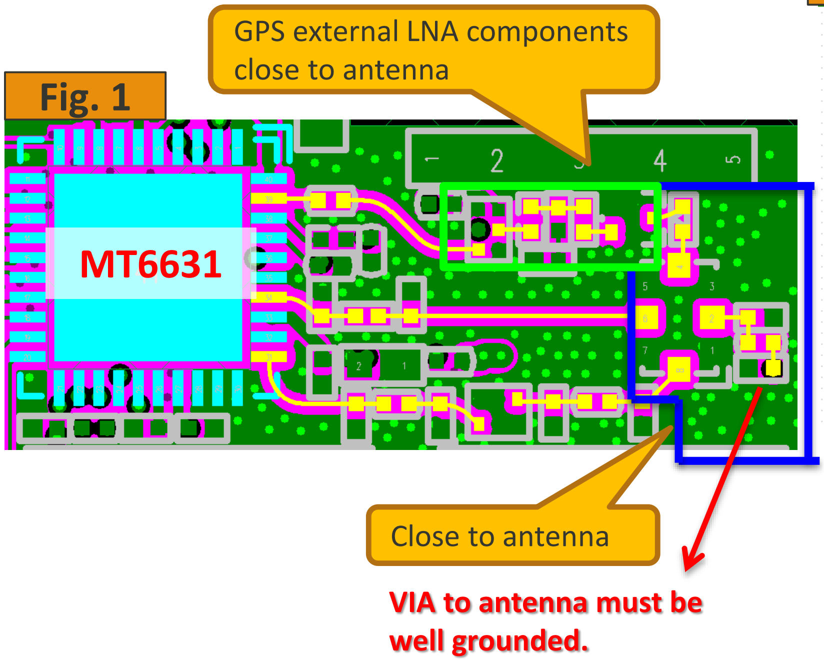
- Connectivity 26MHz (pin 8: XO_IN) should be shielded by GND and routed far away from noise signals.
- 26MHz trace length should be less than 10cm.
- When adding VIA to change layer, keep VIA in every layer well grounded.
- Keep out the metal on L2 and make GND plane on L3 under all crystal circuits.

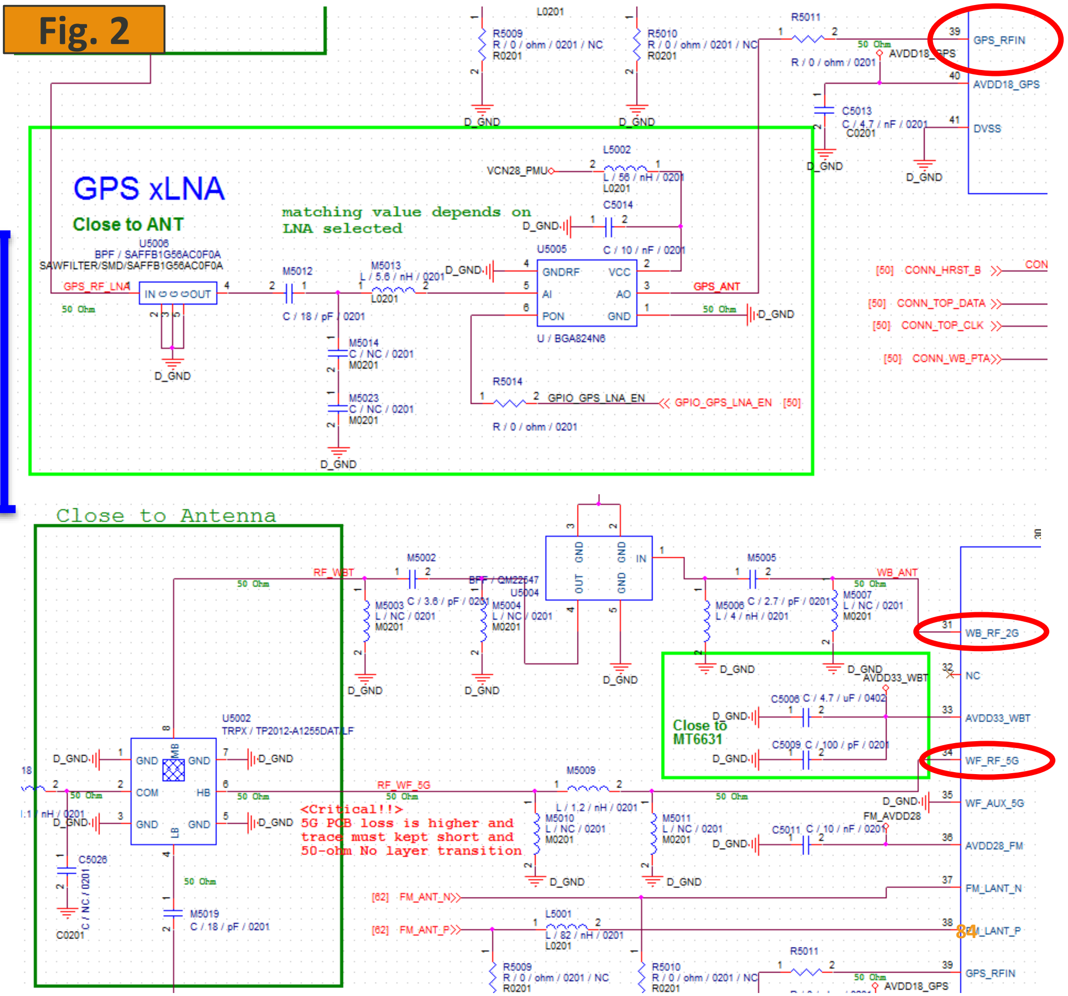




MT6631 RF Trace: WiFi/BT/GPS

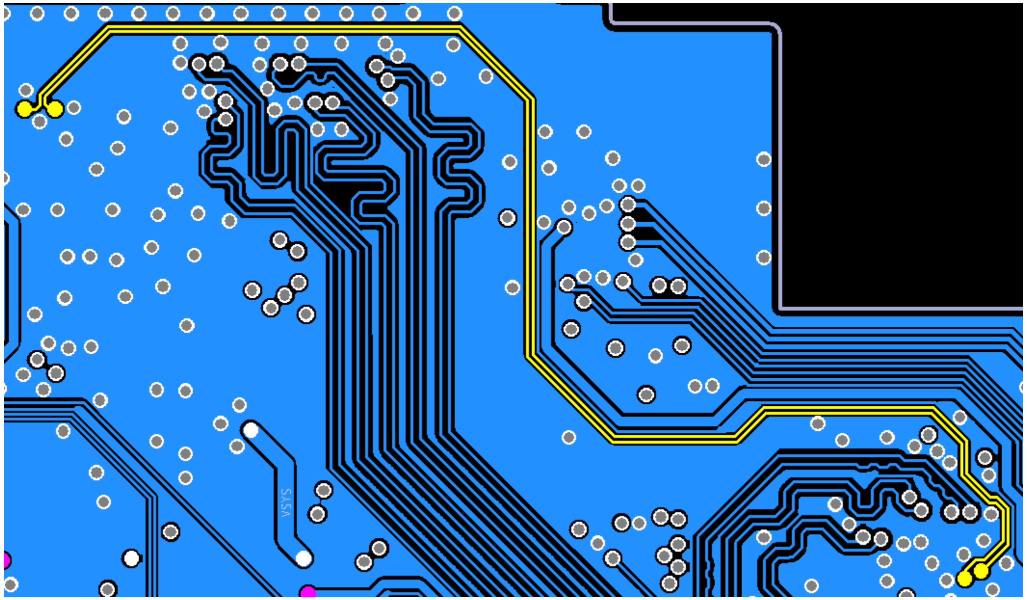
- WB_RF_2G (pin 31), WB_RF_5G (pin 34) and GPS_RFIN (pin 39) are RF antenna pin for WiFi/BT/GPS. Keep **50Ω impedance** with good shielding by GND. (Fig. 1)
- Route on L1 and avoid layer transition for RF trace route (affect impedance control and PCB trace loss). (Fig. 1)
- MT6631 must be placed close to Wi-Fi antenna (make RF trace short, Wi-Fi 5GHz PCB trace loss is huge). (Fig. 1~2)
- GPS external LNA components must be close to antenna and route on Layer 1. (Fig. 1~2)

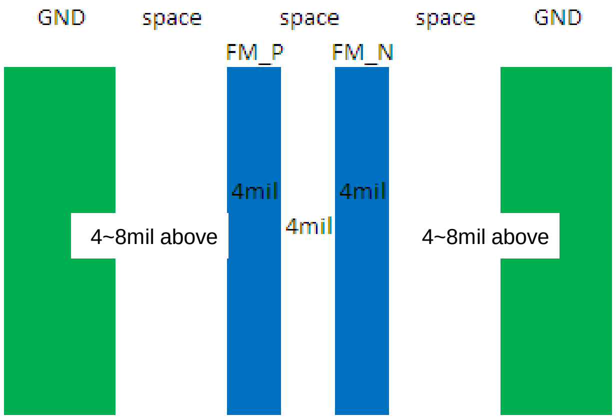


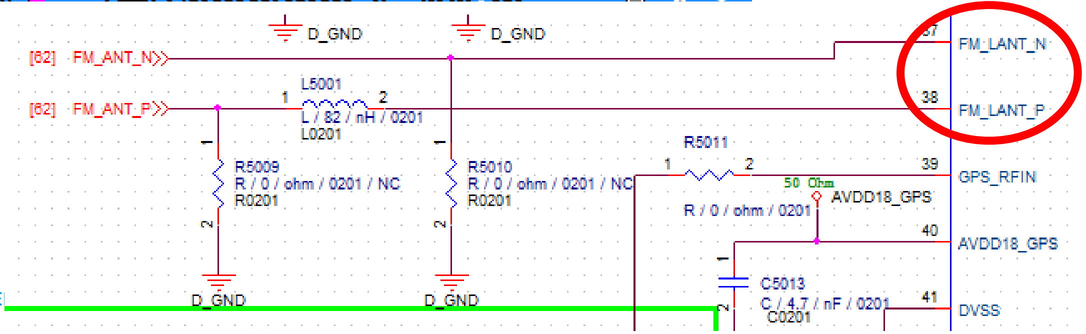


MT6631 RF Trace: FM

- FM_LANT_N (pin 37) and FM_LANT_P (pin 38) are FM signals and required for differential pairs to get better noise immunity.
- FM signals must be shielded by GND (left/right /upper/lower) with stitching GND via.
- If RF trace cannot be well protected, it will produce noise to FM easily.
- ESD interference can be avoided if FM trace is in the inner layer and has good GND shielding.







MT6631 Power Trace (1/2)

- AVDD33_WBT: Place decupling capacitors close to power pin 33. (Fig. 1, 3)
- AVDD28_FM: Place decupling capacitors close to power pin 36. (Fig. 1~2)
- Keep away from other noisy power traces and high speed digital traces.

Fig.1

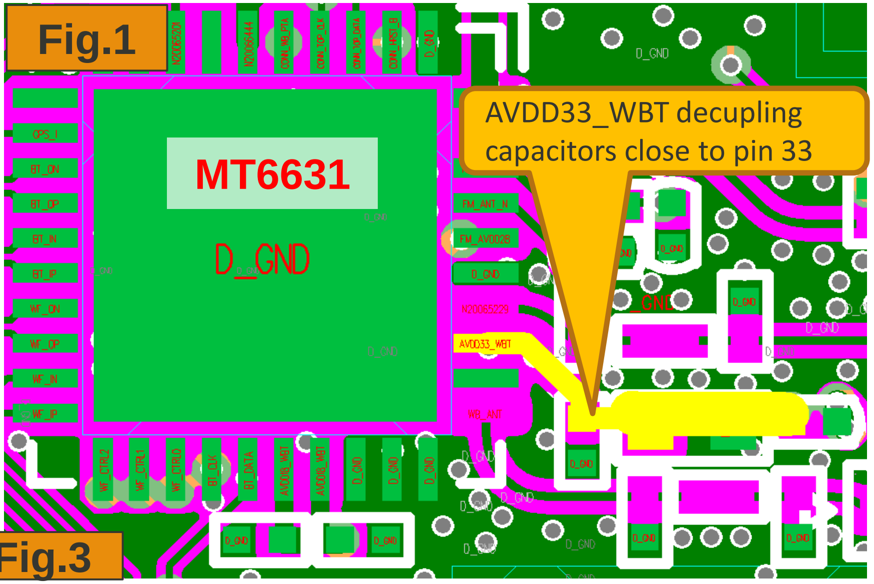


Fig.2

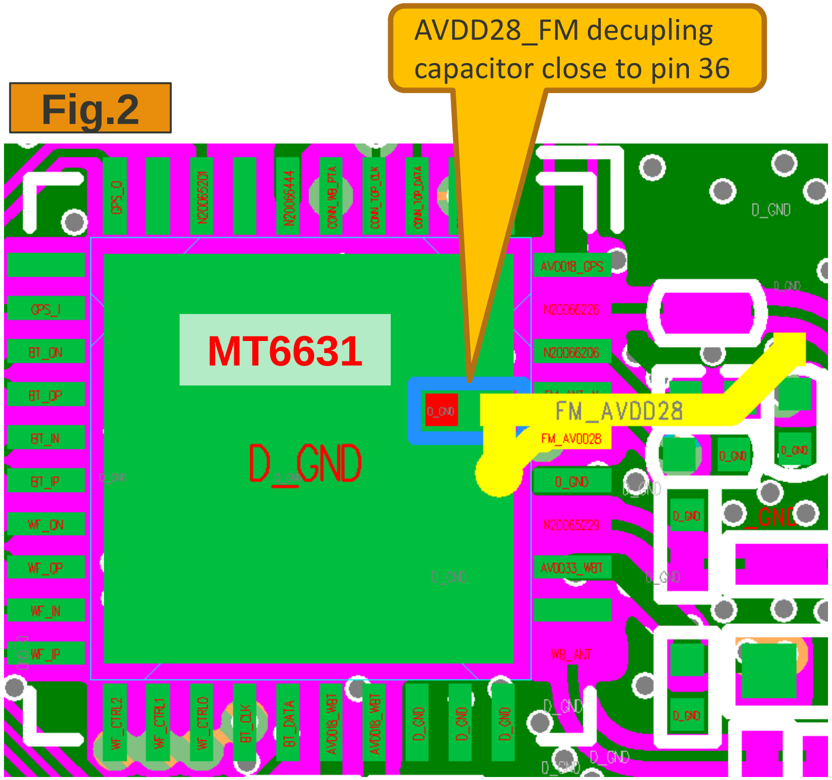
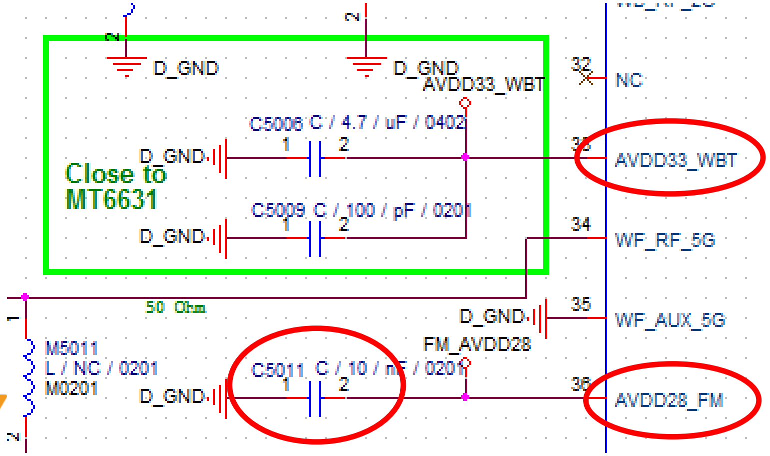


Fig.3



MT6631 Power Trace (2/2)

- AVDD18_WBT: Place decupling capacitors close to power pin 26,27. (Fig.1~2)
- AVDD18_GPS: Place decupling capacitors close to power pin 40. (Fig.1 、3)
- Power traces VCN18_PMU should be used star routing topology to connect AVDD18_WBT (pin 26,27) and AVDD18_GPS (pin 40). (Fig.1)
- Keep away from other noisy power trace and high speed digital trace.

Fig.1

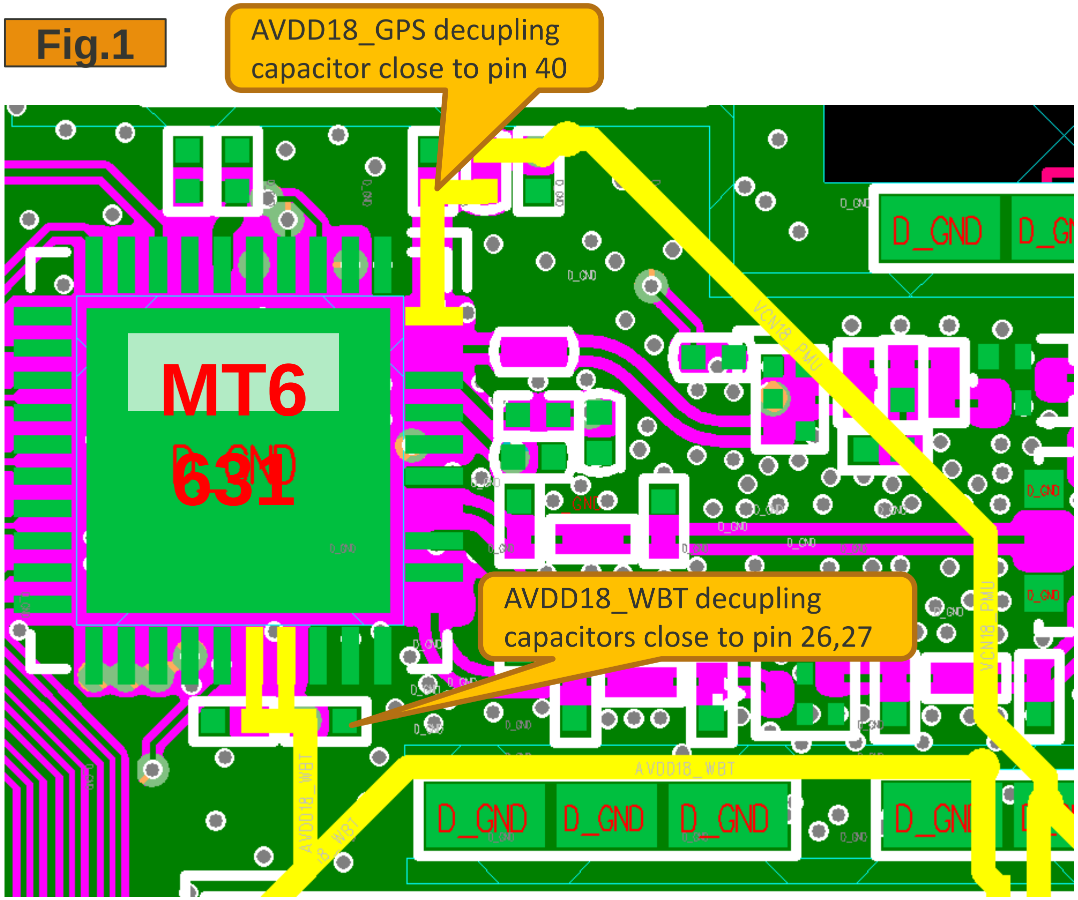


Fig.2

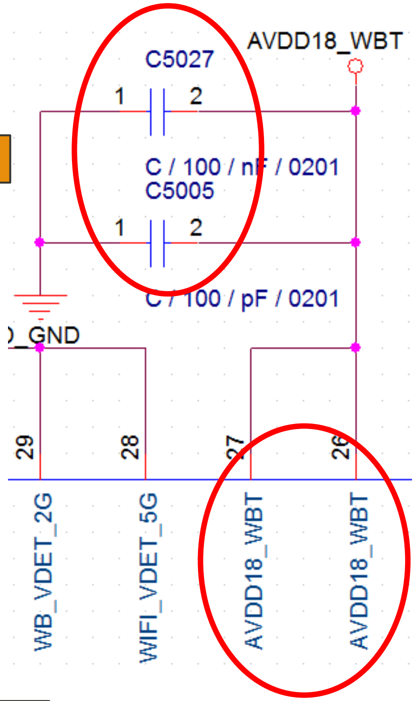
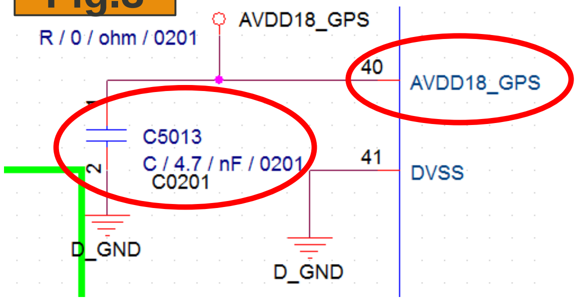


Fig.3



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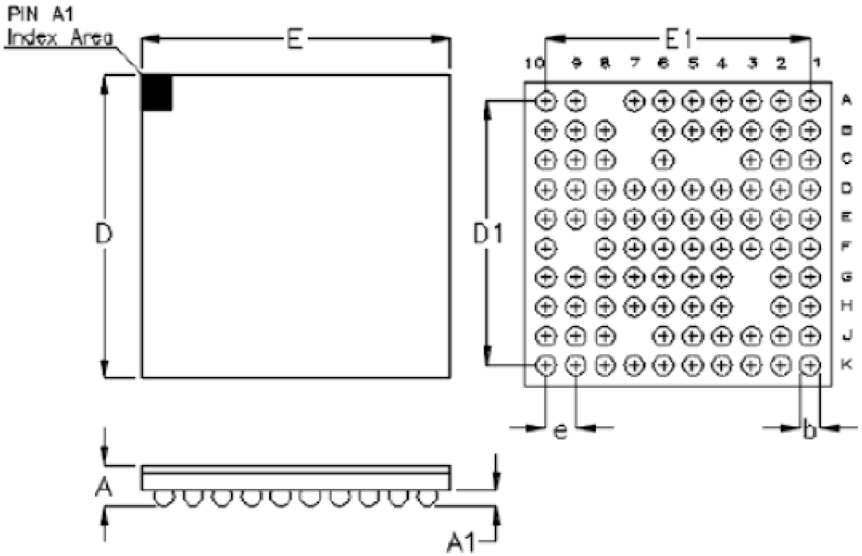
  - MT6371 (battery charger/USB_PD)
  - eMMC/USB/MIPI/SIM card/T-card

MT6371
PCB Layout Guideline

Package Outline of MT6371



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.500	0.600	0.020	0.024
A1	0.170	0.230	0.007	0.009
b	0.240	0.300	0.009	0.012
D	4.100	4.180	0.161	0.165
D1	3.600		0.142	
E	4.180	4.260	0.165	0.168
E1	3.600		0.142	
e	0.400		0.016	

91B WL-CSP 4.22x4.14 Package (BSC)

MT6371 Pin Definition

A1 CHG_VIN	A2 CHG_VIN	A3 CHG_VIN	A4 D-	A5 D+	A6 FL_LEDCS2	A7 FL_LEDCS1		A9 PD_CC2	A10 BL_VLX
B1 CHG_VMID	B2 CHG_VMID	B3 CHG_VMID	B4 FL_VMID	B5 FL_VMID	B6 FL_VMID		B8 PD_IRQB	B9 PD_VCONN5V	B10 BL_PGND
C1 CHG_VLX	C2 CHG_VLX	C3 CHG_VLX			C6 FL_VINTORCH		C8 CHG_ILIM	C9 PD_CC1	C10 BL_VDDA
D1 CHG_PGND	D2 CHG_PGND	D3 CHG_PGND	D4 CHG_BOOT	D5 VBATS	D6 FL_STROBE	D7 FL_TORCH	D8 CHG_OTG	D9 BL_VOUT	D10 BL_LED1
E1 VSYS	E2 VBUS	E3 CHG_VDDP	E4 OVP_CTRL	E5 AGND	E6 AGND	E7 AGND	E8 CHG_QONB	E9 CHG_ENB	E10 BL_LED2
F1 VSYS	F2 VSYS	F3 CHG_VBATOVPB	F4 NC	F5 AGND	F6 AGND	F7 AGND	F8 CHG_DSEL		F10 BL_LED3
G1 VBAT	G2 VBAT		G4 CHG_STAT	G5 AGND	G6 AGND	G7 AGND	G8 FL_TXMASK	G9 AGND	G10 BL_LED4
H1 VBAT	H2 VBAT		H4 RGB_ISINK4	H5 RGB_ISINK1	H6 DB_ENN	H7 DB_ENP	H8 MRSTB	H9 BL_PWM	H10 BL_EN
J1 LDO_VOUT	J2 LDO_VIN	J3 TS	J4 RGB_ISINK3	J5 RGB_ISINK2	J6 IRQB		J8 SCL	J9 SDA	J10 VDDA
K1 DB_NEGVOUT	K2 DB_NEGCF2	K3 DB_NEGPGND	K4 DB_NEGCF1	K5 DB_POSVOUT	K6 DB_BSTVOUT	K7 DB_POSVLX	K8 DB_POSPGND	K9 VDDM	K10 DB_VDDA

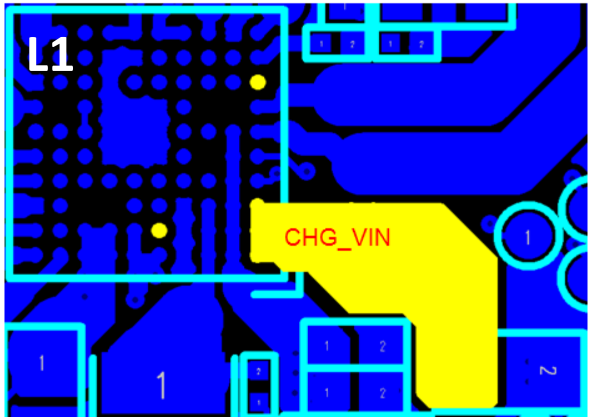
Figure 1-1. MT6371 WL-CSP-91B 4.22x4.14 (BSC) (top view)

MT6371 Schematic/Layout Notice

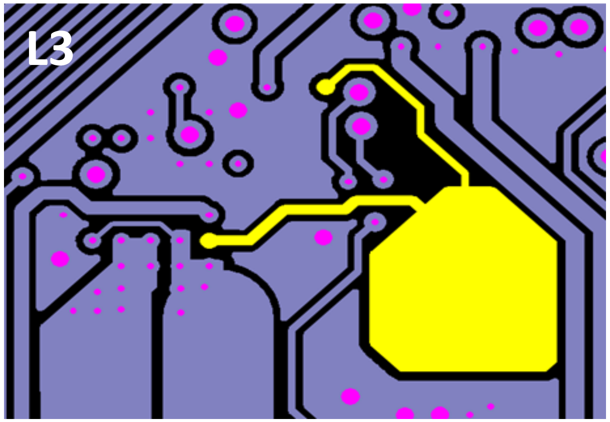
- High current path must enlarge trace width as 25mil/1A.
  - CHG_VIN, CHG_VLX, VSYS and VBAT → 4A
  - CHG_VMID, FL_VMID → 2.5A
  - FLED1/2 → 1.5A
- Bypass CAP/Resistor near to related ball.
  - VDDM, VDDA, BL_VDDA, DB_VDDA, CHG_BOOT to CHG_VLX, and CHG_ILIM.
- Inductor close to LX pins and not couple to other sensitive traces (e.g. SDA/SCL)
- VDDM and VDDA, BL_VDDA and DB_VDDA cap's GND should be directly connected to GND plane.

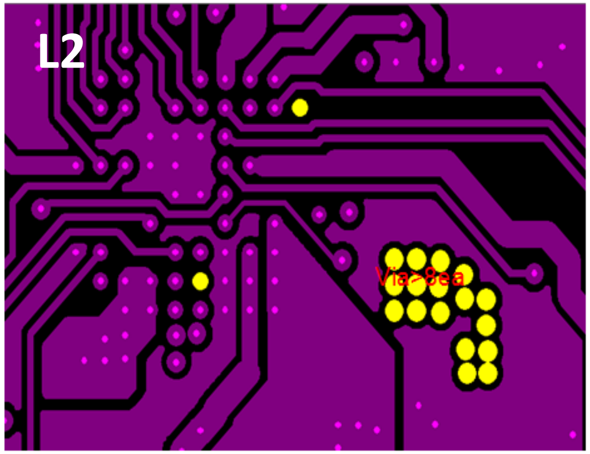
MT6371 - Charger CHG_VIN Trace

- High current path CHG_VIN, CHG_VLX, VSYS and VBAT → 4A

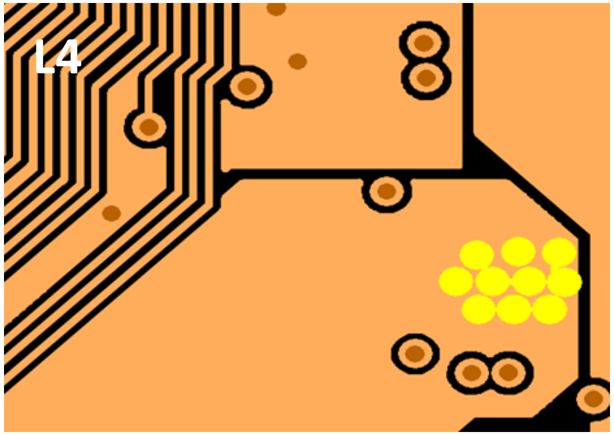


L1: CHG_VIN trace must be > 2.5mm



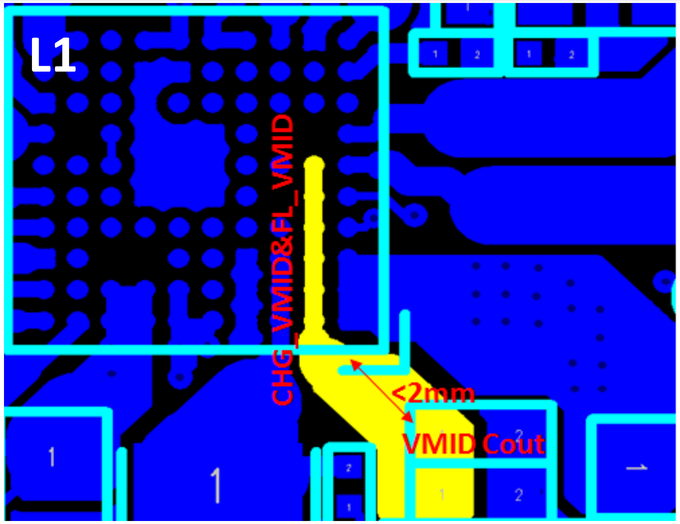


L2: Via numbers should be > 8ea for current path.

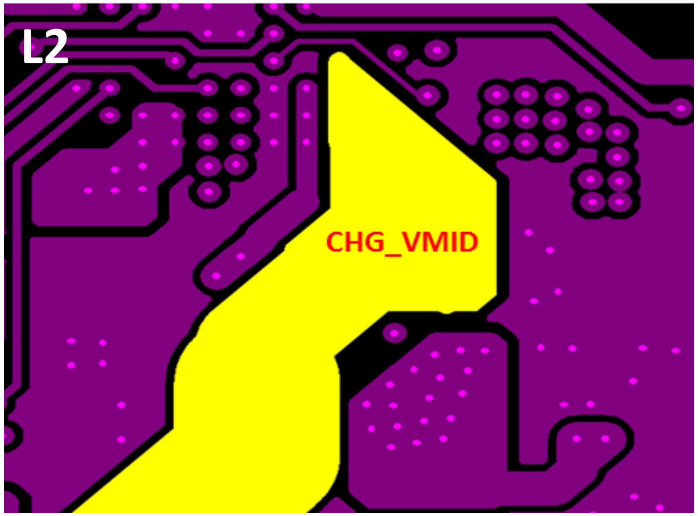


L4: CHG_VIN trace must be > 2.5mm

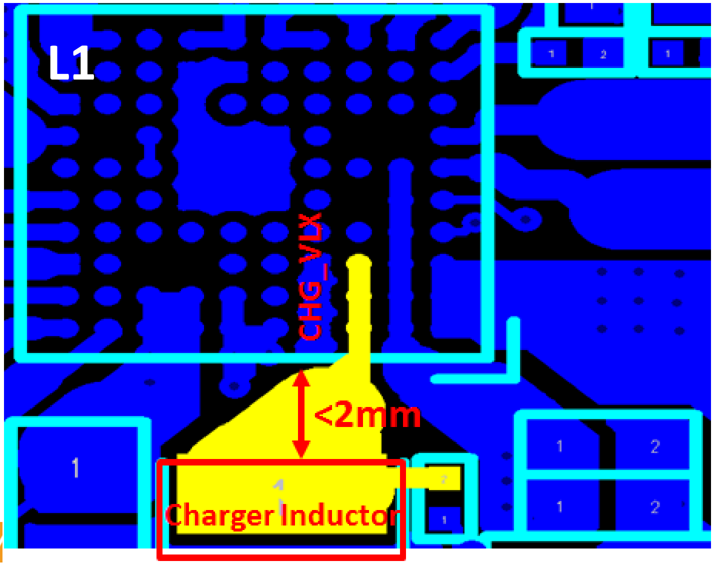
MT6371 - Charger CHG_VMID & CHG_VLX



CHG_VMID Output Cap
place as close to IC (<2mm)

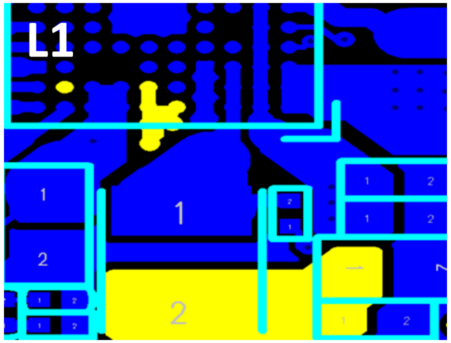


CHG_VMID (=FL_VMID) trace must be > 1.5mm
for parallel charger application

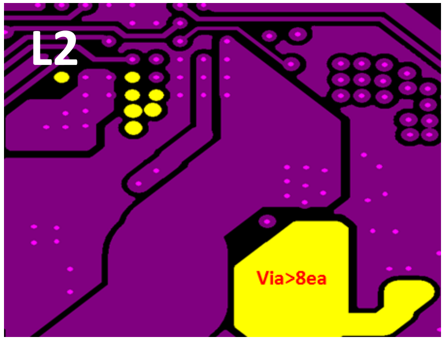


CHG_VLX Inductor
place as close as possible to IC (<2mm)

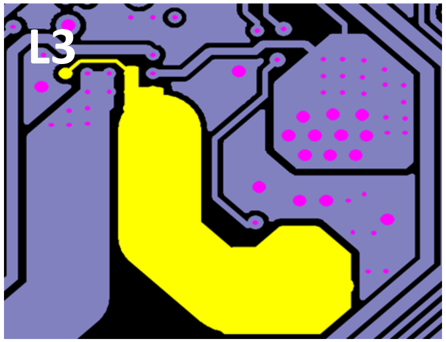
MT6371 – VSYS & VBAT



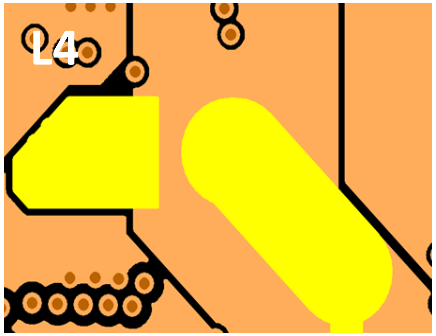
VSYS trace
must be > 2.5mm



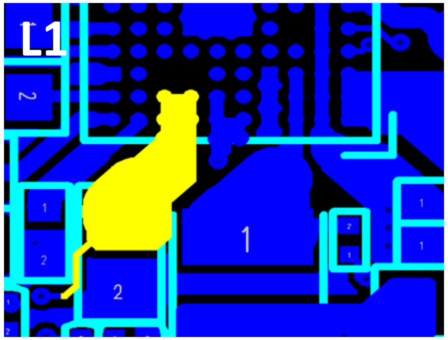
VSYS-Via should be >
8ea for current path.



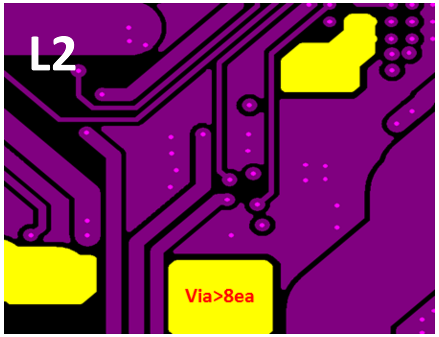
VSYS trace
must be > 2.5mm



VSYS trace
must be > 2.5mm



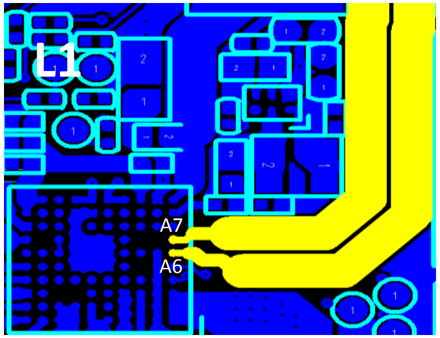
VBAT trace
must be > 2.5mm



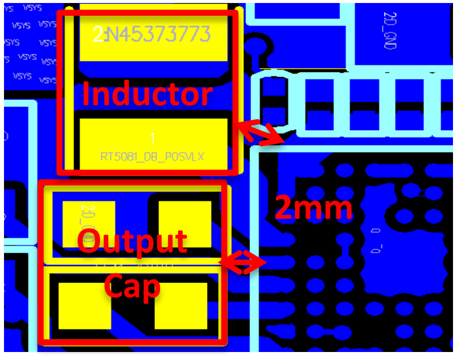
VBAT-Via should be >
8ea for current path.

VBAT trace
must be > 2.5mm

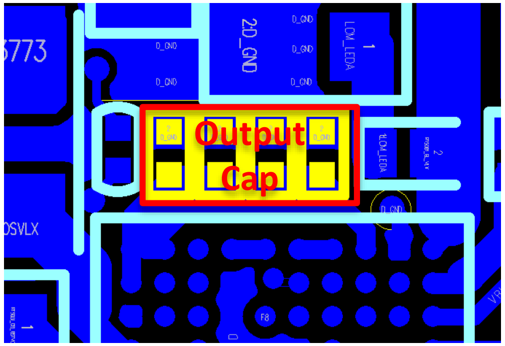
MT6371 – FLED/Display/VDDM



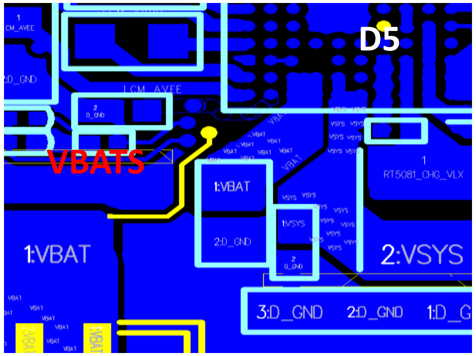
FLED1/FLED2 (Pin: A6,A7)
trace must be > 750um



Display Bias (Pin: K7)
Inductor and Output Cap
Close to IC < 2mm



VDDM/VDA
Output Cap Close to IC < 2mm
These output caps' GND should be isolated from the nearby GND trace and plane then connected to main GND directly.



VBATS (Pin: D5) sense trace
must connect to VBAT - battery pack side

Outlines

- **Packaging**
  - Package outline of MT6765
  - MT6765 footprint recommendation
  - MT6765 ball out design
- **General Guidelines**
  - PCB stack-up recommendation
  - Placement notes
- **Design Guidelines for High-speed Digital Signals**
  - LPDDR4X
  - PDN design
- **Others**
  - MT6765 RF interface - MT6177 (RF transceiver)
  - MT6765 RF interface - MT6177M (RF transceiver)
  - MT6357 (PMU)
  - MT6631 (BT/FM/Wi-Fi/GPS)
  - MT6371 (battery charger/USB_PD)
  - eMMC/USB/MIPI/SIM card/T-card

eMMC/USB/MIPI/
SIM Card/T-Card/MSDC

eMMC 5.x

BreakOut Region Topology:

Main routing on L1/L3, L2/L4 solid reference gnd:

Breakout length ≦ 3810 um (as short as possible)

A. Keep L2 as solid reference gnd as possible.
B. Place the gnd stitching via between BGA ball and L2 gnd on both AP/eMMC.
C. Trace Width (w) = Minimum Trace Width
D. Trace Spacing ≧ W um

Main Route Region Topology:

Main routing on L1/L3, L2/L4 solid reference gnd:

Trace length <=50800 um

A. Trace Width (w) = W um
B. Trace Spacing:
   1. DATA to DATA ≧ 2Wum
   2. CLK to DATA/CMD/DSL/RST ≧ 2W um
   3. DSL to DATA/CMD/CLK/RST ≧ 2W um
   4. CMD to DATA/CLK/DSL/RST ≧ 2W um
   5. RST to DATA/CLK/DSL/CMD ≧ 2W um

Length matching:

A. |Clock – Data/CMD| ≦ 7620 um
B. |DSL – Data/CMD| ≦ 7620 um

PI : PCB Decap location

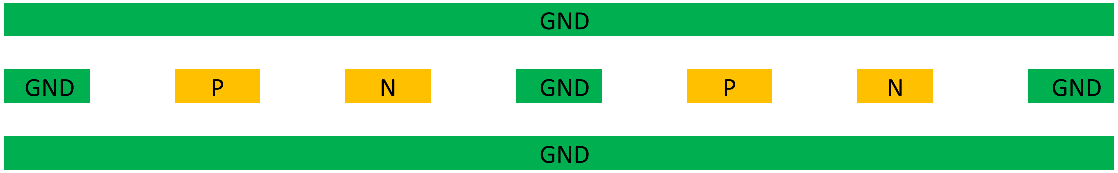
A. Distance to SOC ≦ 3810 um
B. Trace width (W) ≧ 200 um
C. Cap Value ≧ 0.1 uF

USB 2.0

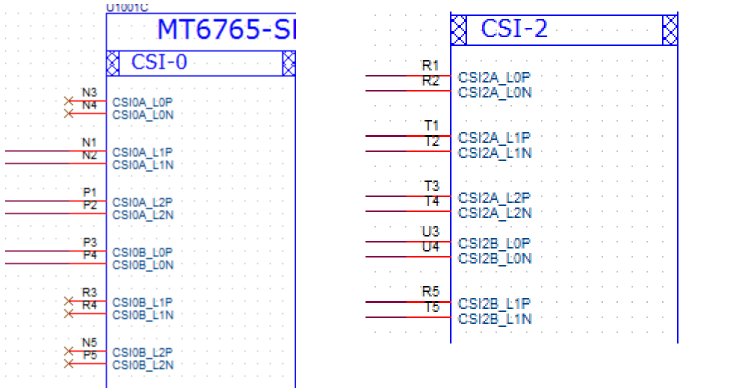
- Differential pairs are well-shielded by GND and GND vias (adjacent and up/down layers).
- Routing differential pair straight and symmetrically on the same layer.
- USB2.0: Maximum of 2 via-hole/layer change.

	Differential impedance	P/N skew	Total length*
USB_DP/DM	90ohm	< 1500um	< 8inch if trace only

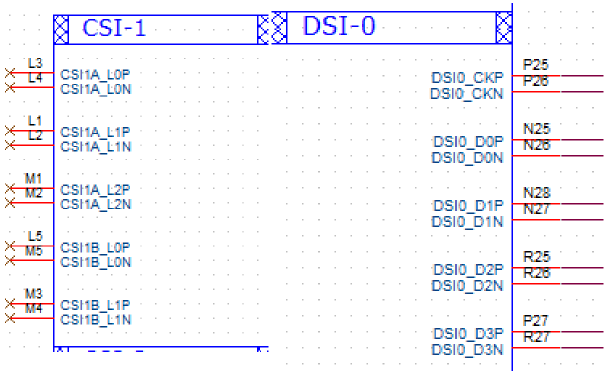
* If there is switch/FPC for USB 2.0, keep IL < 2dB @ 240MHz



MIPI



- MIPI signals' differential impedance: 100Ω
- Total length < 6 inch (PCB + FPC + Module)
  - Lane-to-clock matching ≤ 2.5mm
  - P/N skew: ≤ 0.625mm for > 1.5Gbps
≤ 1.5mm for ≤ 1.5Gbps



- Well shielded by GND (adjacent and up/down layers) is recommended; otherwise keep the spacing ≧ 3x min (h1, h2) rule. (Fig. 1&2)
- CMMCLK: Well shielded by GND (adjacent and up/down layers)
- Ground via should be closed to signal via when there is layer transition, < 150mil

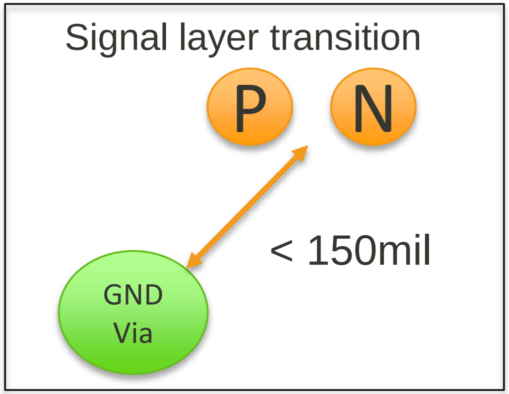


Fig.1

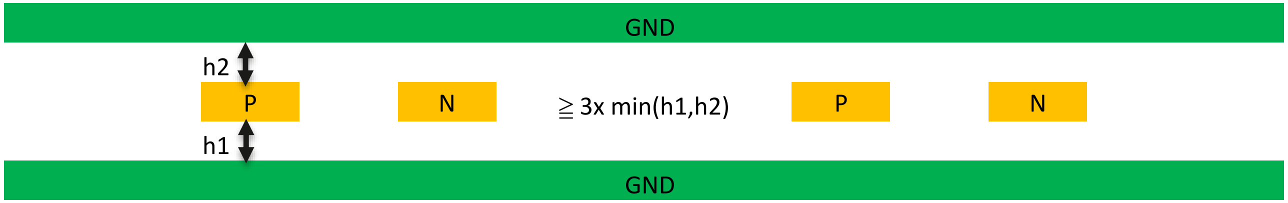
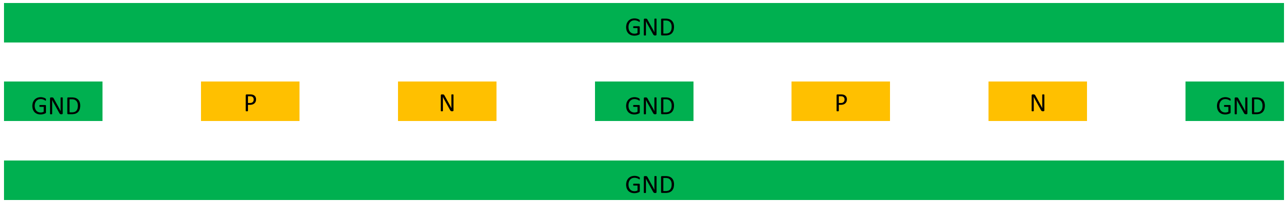
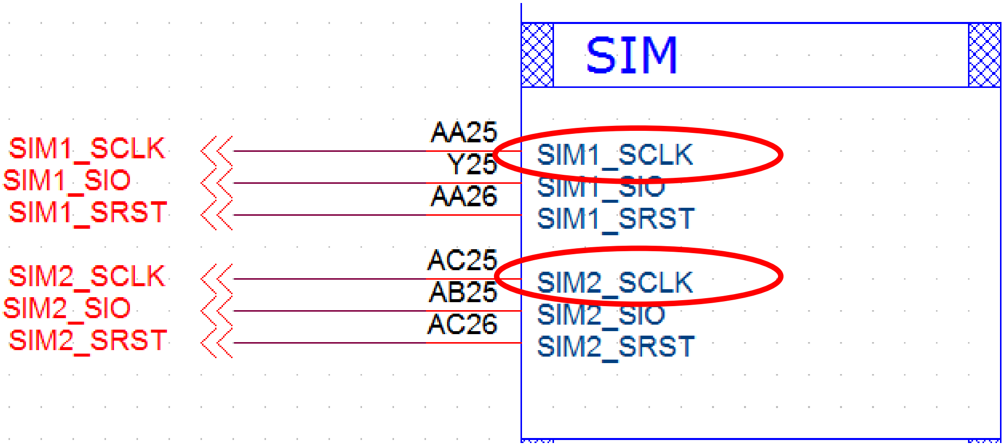


Fig.2



SIM Card

SIM1_SCLK/ SIM2_SCLK should be shielded by GND.



MSDC1 T-Card

Break Out Region Topology:

Main routing on L1/L3, **L2/L4 solid reference GND**:

<u>Breakout length ≦ 300mil (as short as possible)</u>

A. Keep L2 as solid reference GNN as possible.
B. Place the gnd stitching via between BGA ball and L2 gnd on both AP/eMMC.
C. Trace width (W) = Minimum trace width
D. Trace spacing ≧ W mil

Main Route Region Topology:

Main routing on L1/L3, **L2/L4 solid reference GND:**

<u>Trace length <= 4000mil</u>

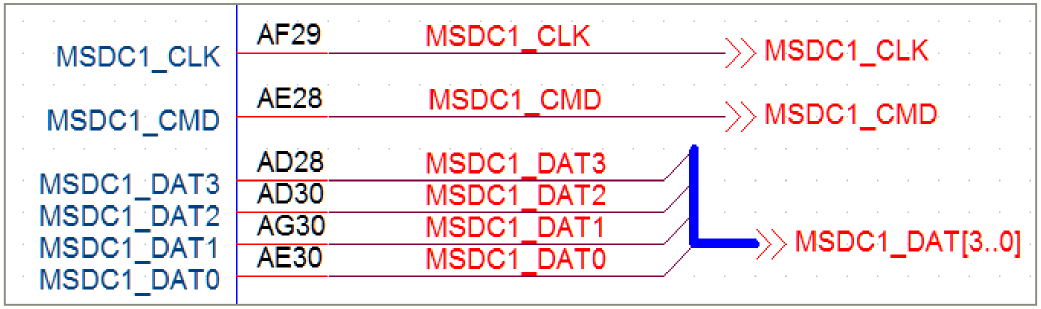
A. Trace width (w) = W mil
B. Trace spacing:
   1. DATA to DATA ≧ W mil, 4 trace shielding w/gnd
   2. CLK shielding w/GND on both side
   3. CMD shielding w/GND on both side

Length matching:

A. |Clock – Data/CMD| ≦ 300mil

PI : PCB Decap location

A. Distance to SOC ≦ 150mil
B. Trace width (W) ≧ 8mil
C. Cap Value ≧ 0.1 uF



MEDIATEK

everyday genius

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